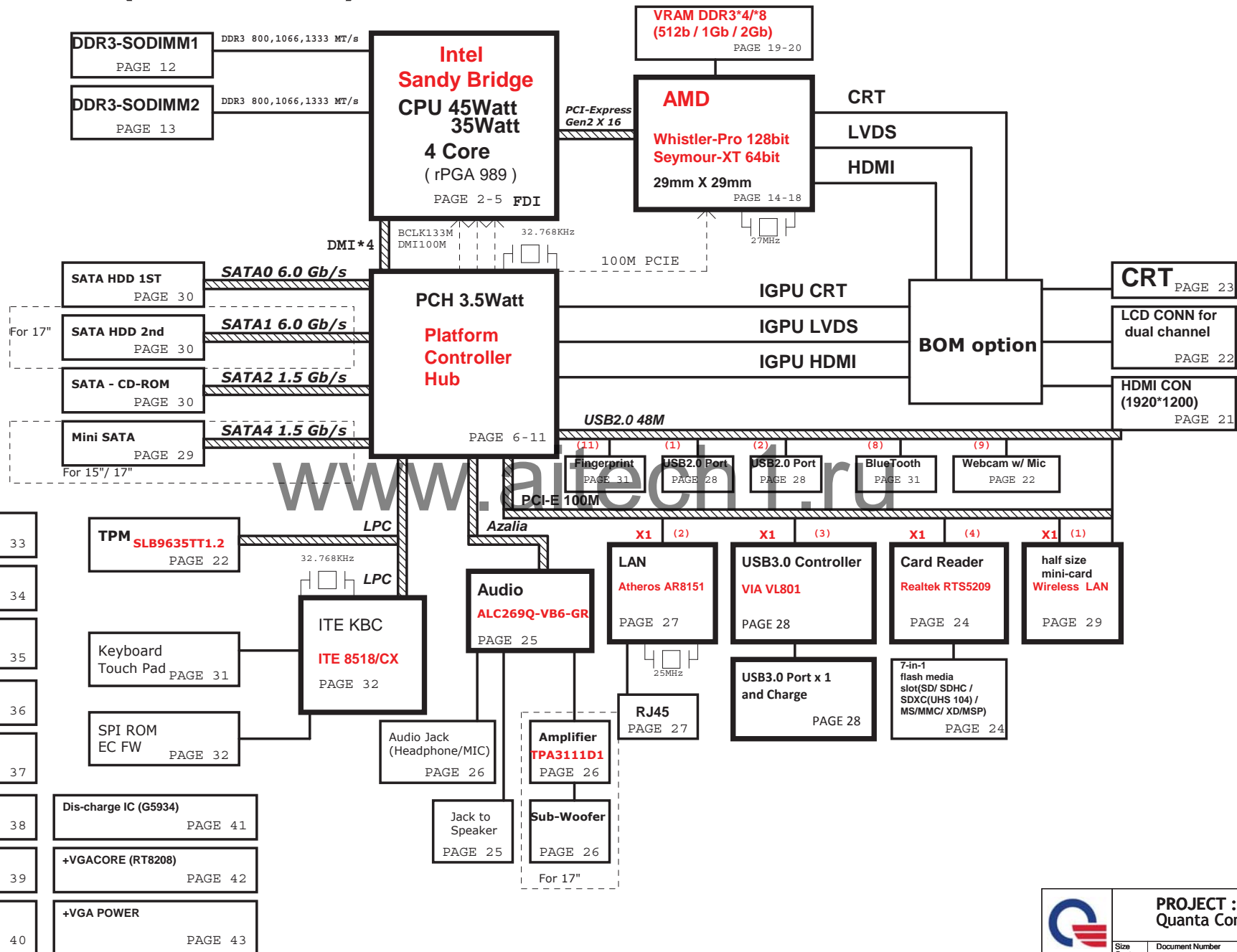
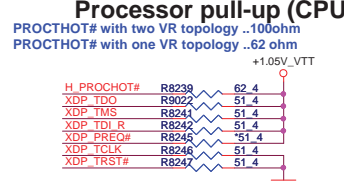
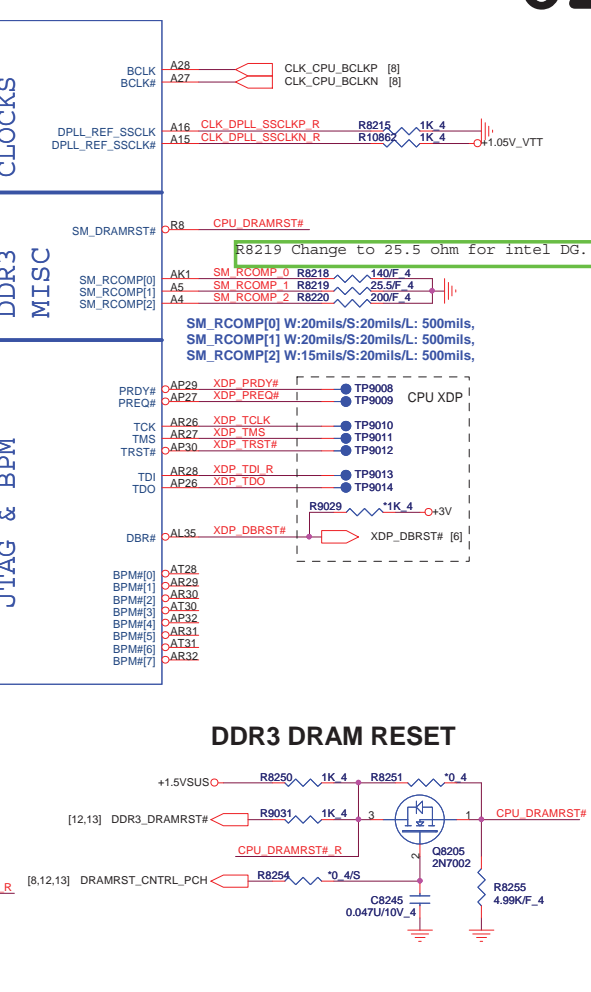


LG2/4 (14"/15.6") MUXLESS and Dis. BLOCK DIAGRAM 01

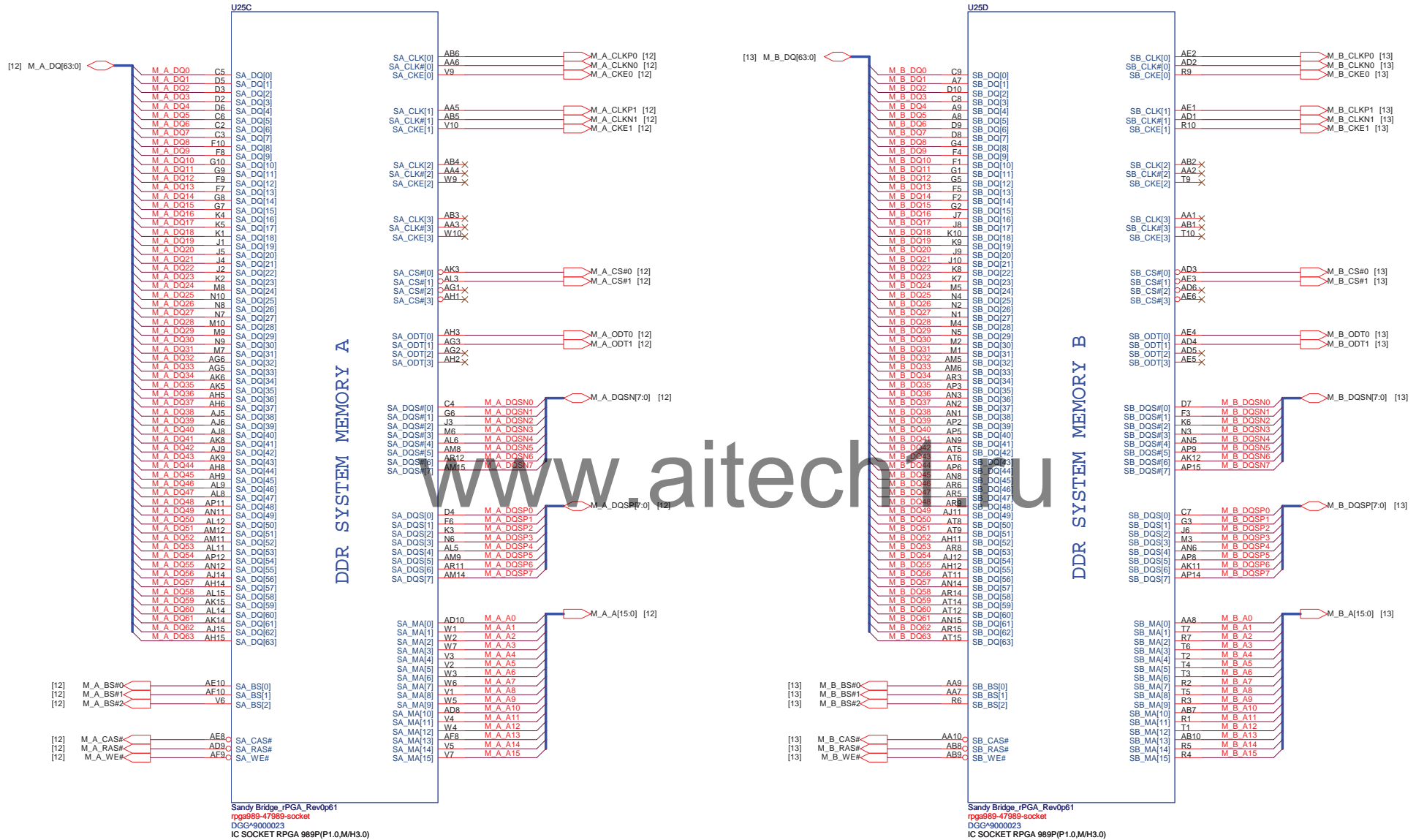
PCB 8L STACK UP

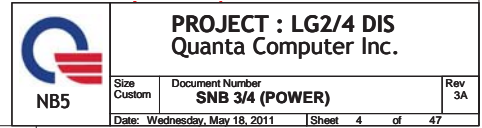
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT



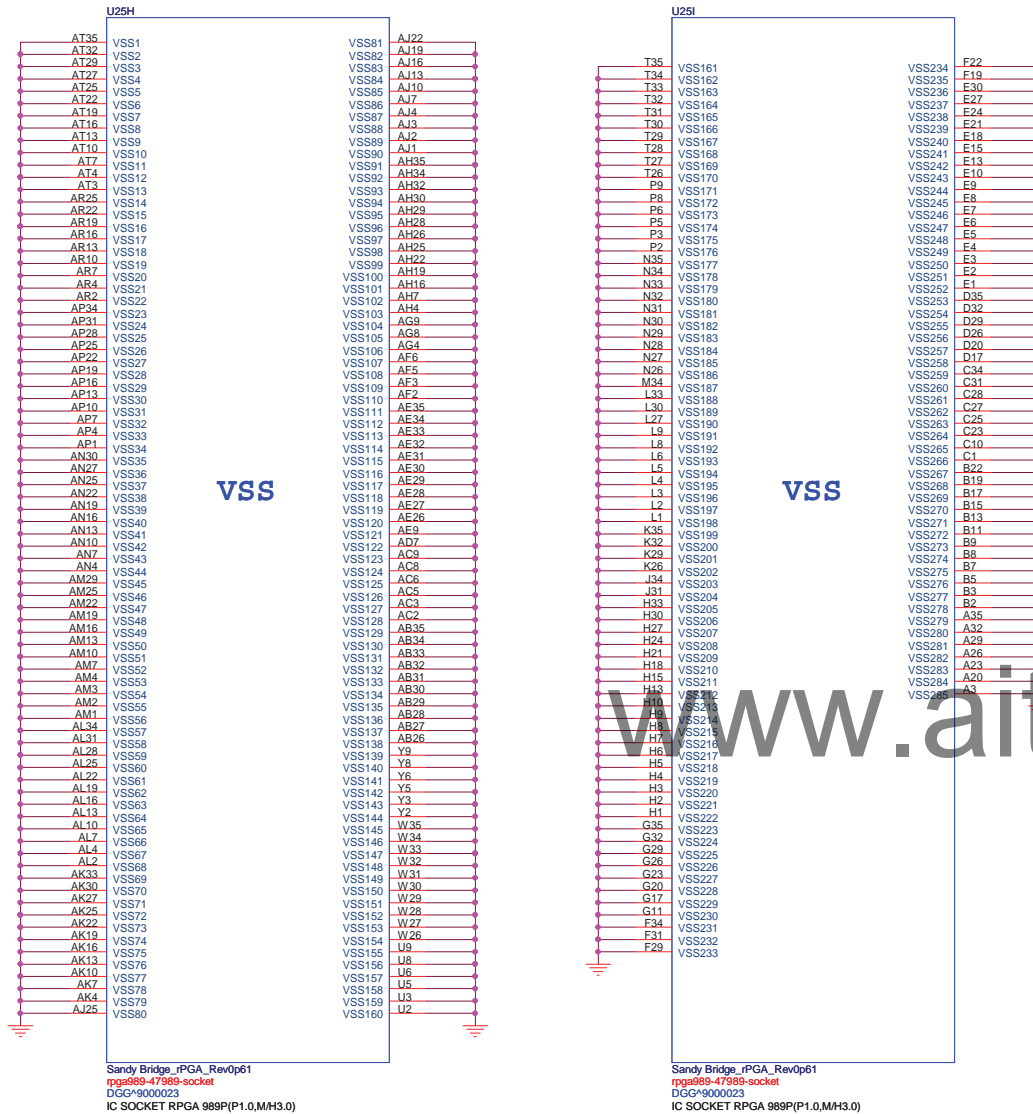


Sandy Bridge Processor (DDR3)

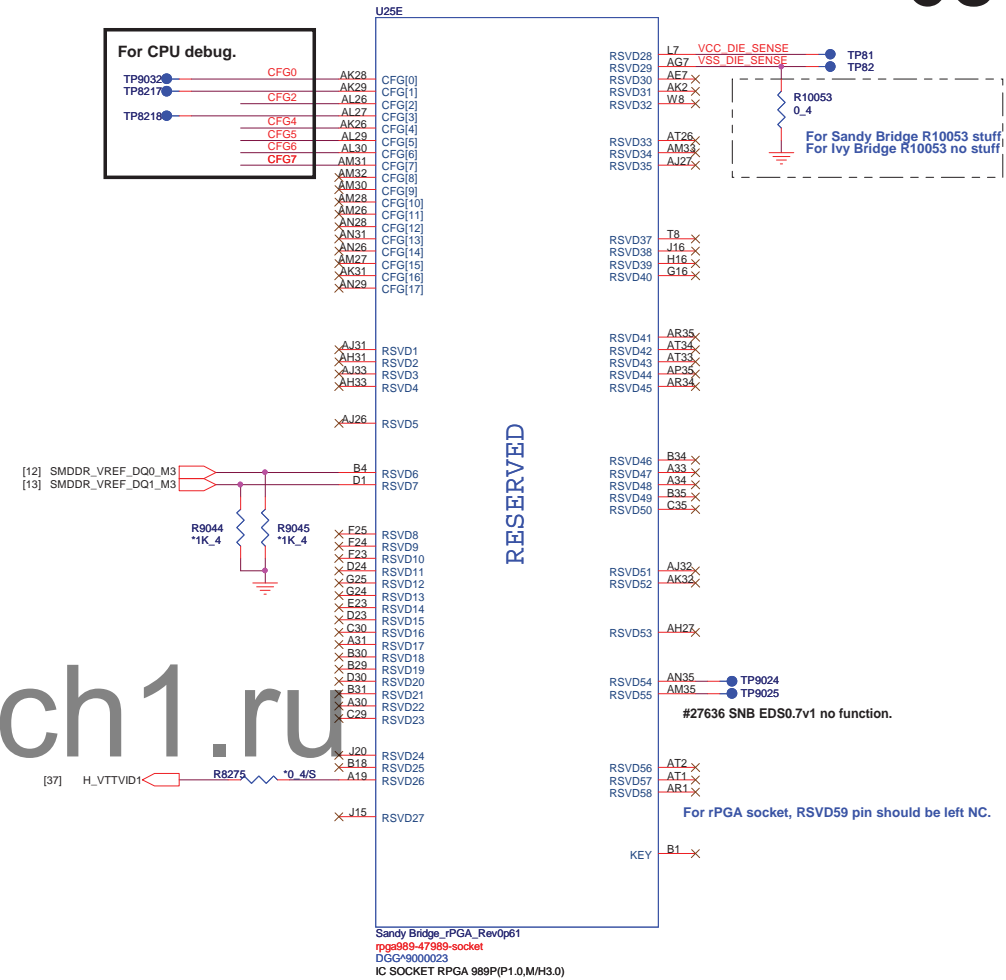




Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



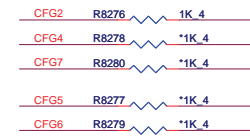
Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

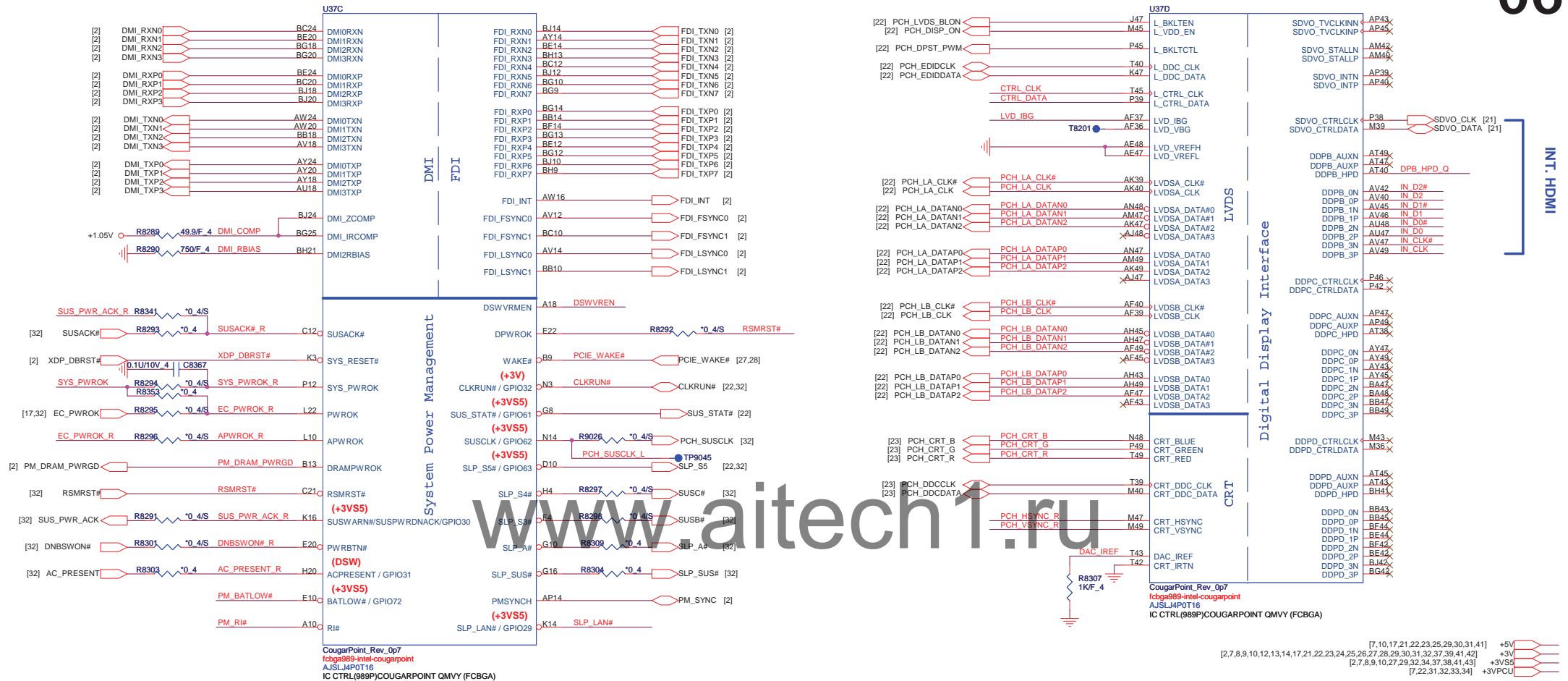
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 4/4 (GND)	3A
Date: Thursday, May 19, 2011	Sheet 5 of 47	

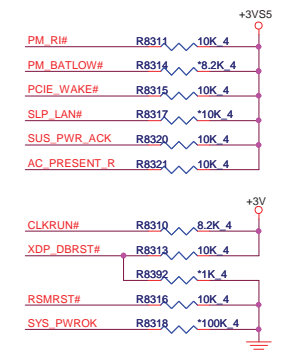


PCH Pull-high/low(CLG)

INT LVDS & CRT disable
(DIS only remove)

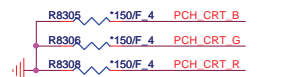
INT HDMI disable (DIS only remove)

System PWR_OK(CLG)

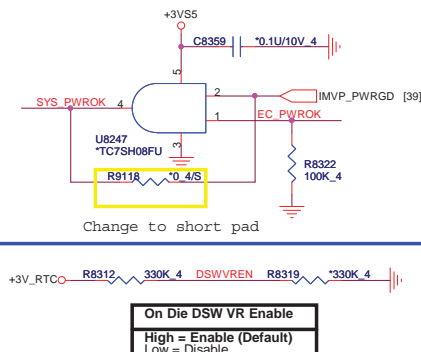
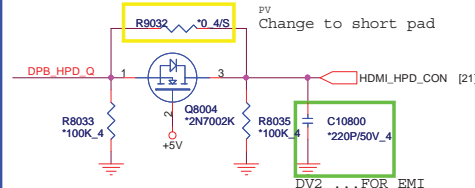


PD Res place close to PCH

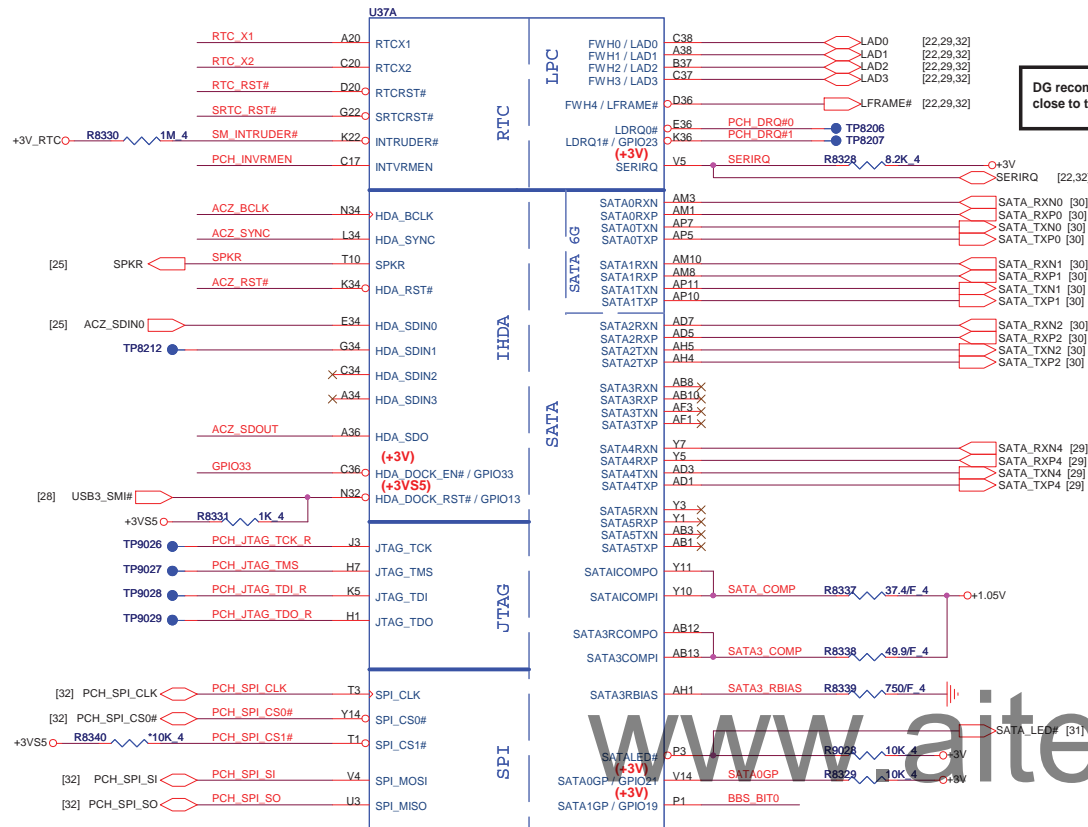
PCH to Res routing 50 ohm Impedance.
Res to connector filter routing 37.5ohm Impedance.



INT HDMI Detect Function



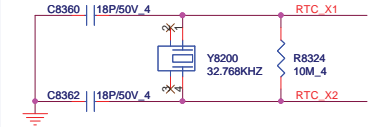
Cougar Point (HDA, JTAG, SATA)



DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

RTC Clock 32.768KHz

07



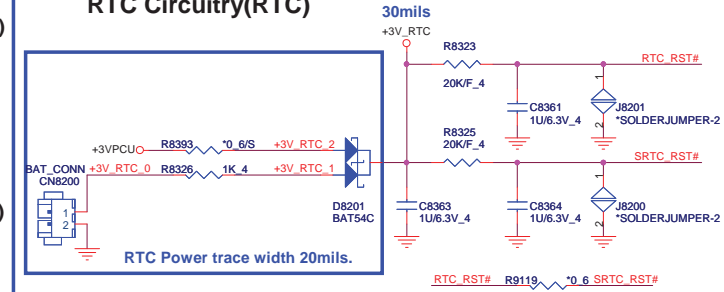
HDD0 (SATA3 6.0Gb/s)

2nd HDD0 (SATA3 6.0Gb/s)

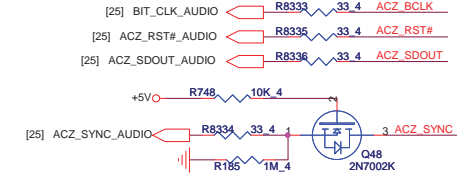
ODD

MINISATA (SATA1 1.5Gb/s)

RTC Circuitry(RTC)

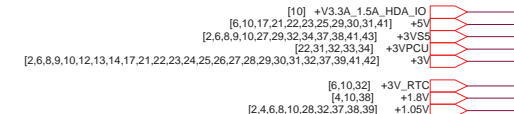


HDA Bus(CLG)

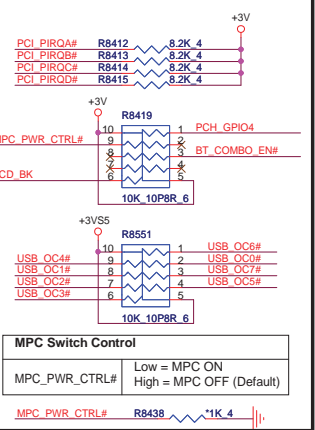


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R8349 1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R8350 1K 4 R9138 10K 4 +3V PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R8351 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R8355 1K 4 ACZ_SDOA [32]
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R8358 1K 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R8357 1K 4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R8359 1K 4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R8360 2.2K 4 R8361 1K 4 NV_CLE [8] H_SNB_IVB# [2]
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R9148 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	[32] ACZ_SDOA ACZ_SDOA R8362 1K 4 +3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R8365 1K 4 ICC_EN# [9]
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R8366 1K 4 PLL_ODVR_EN [9]
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R8398 1K 4 +3V



PCI/USB0# Pull-up(CLG)



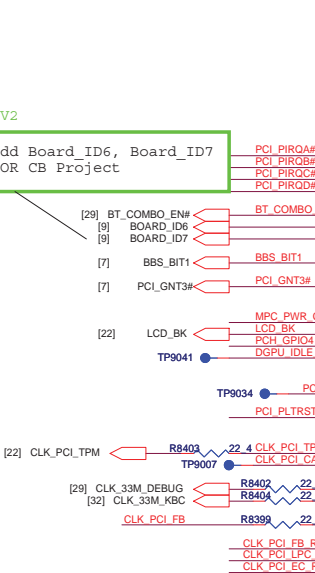
MPC Switch Control

MPC_PWR_CTRL# Low = MPC ON
High = MPC OFF (Default)

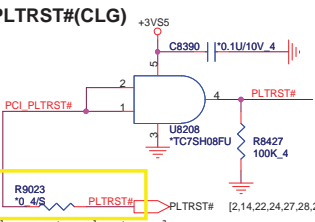
MPC_PWR_CTRL# R8438 *1K 4

DPV2

Add Board_ID6, Board_ID7
FOR CB Project

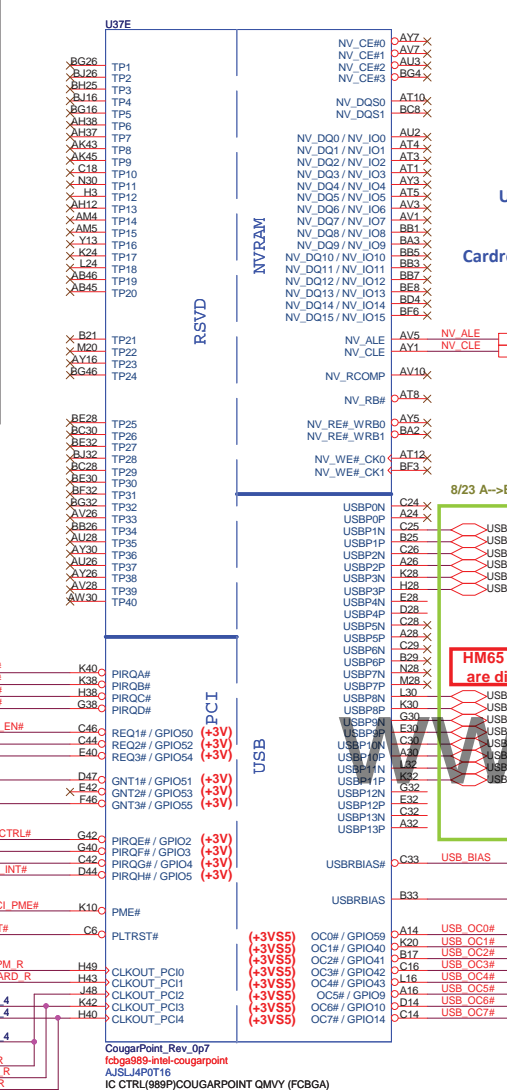


PLTRST#(CLG)



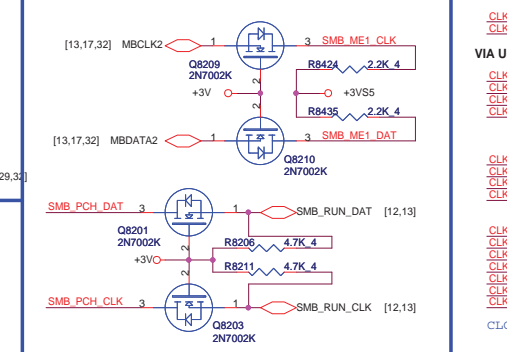
Change to short pad

Cougar Point-M (PCI,USB,NVRAM)



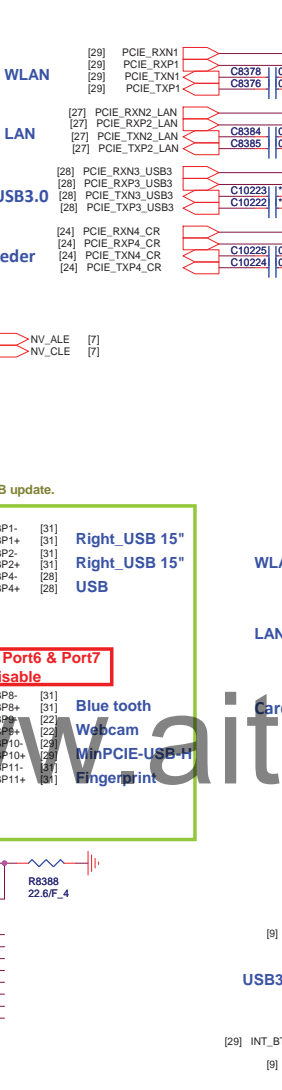
CougarPoint_Rev.07
fcbg989-intel-cougarpoint
AJSLJAP0T16
IC CTRL(989P)COUGARPOINT QMYY (FCBGA)

SMBus/Pull-up(CLG)

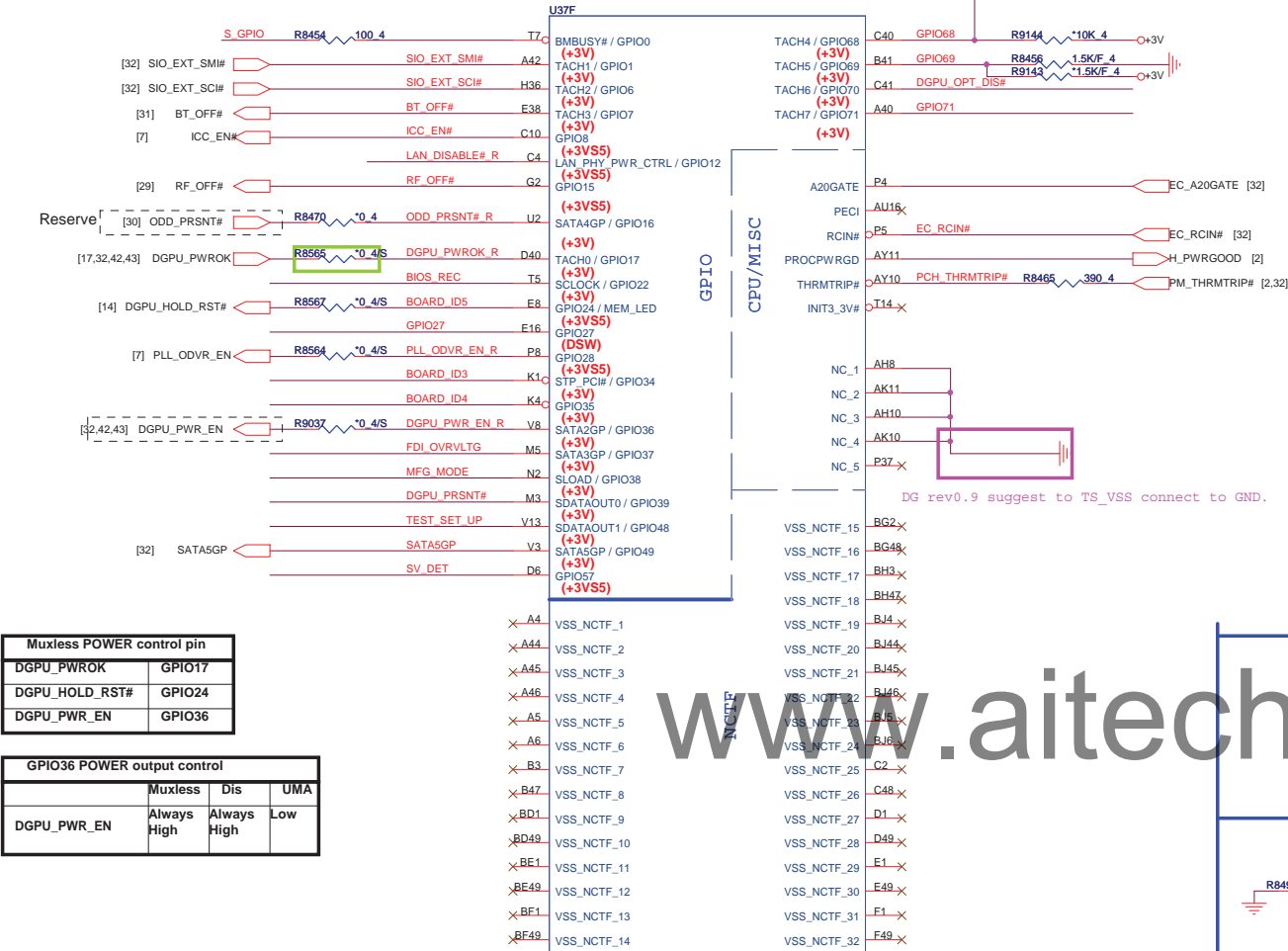


CLOCK TERMINATION for FCIM

Cougar Point-M (PCI-E,SMBUS,CLK)



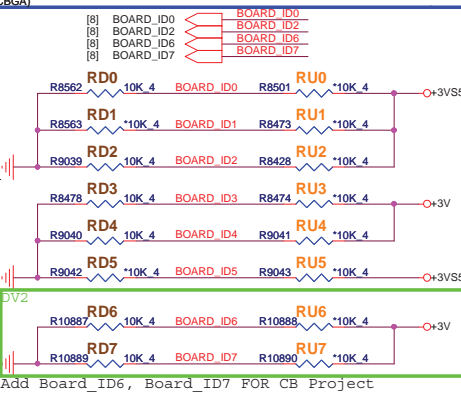
Cougar Point (GPIO,VSS_NCTF,RSVD)



Muxless POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

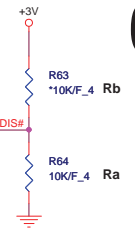
GPIO36 POWER output control			
	Muxless	Dis	UMA
DGPU_PWR_EN	Always High	Always High	Low

BOARD ID SETTING									
Board ID	ID0	ID1	ID2	ID3	ID4	ID6	ID7	GPIO70	GPIO39
LG/CB	0=LG 1=CB								
15.6" / 14"			14"15" 17"	LG6					
			ID2	1 0 0 1					
17"			ID3	0 0 1 1					
doby					1=YES 0=NO				
DIS/Muxless								1= Muxless 0=DIS	
UMA/VGA								1= VGA 0=UMA	

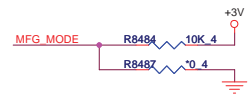


	Ra	Rb
UMA/Muxless	NC	Stuff
DIS	Stuff	NC

DGPU_OPT_DIS#:
High : Muxless.
Low: Discrete.



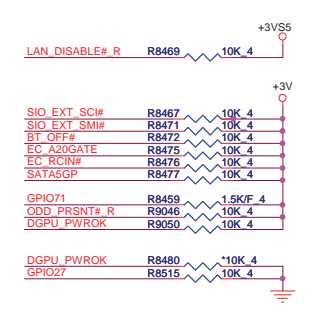
MFG-TEST



SGPIO



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TIS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY	
High = Disable (Default)	Low = Enable

TEST SET UP	
High = Strong (Default)	

TEST DETECT	
Low = Default	

DMI TERMINATION VOLTAGE OVERRIDE	
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)	

FDI TERMINATION VOLTAGE OVERRIDE	
LOW - Tx, Rx terminated to same voltage	

GFX Present

	DIS/Muxless	UMA
Stuff	Ra	Rb
NC	Rb	Ra

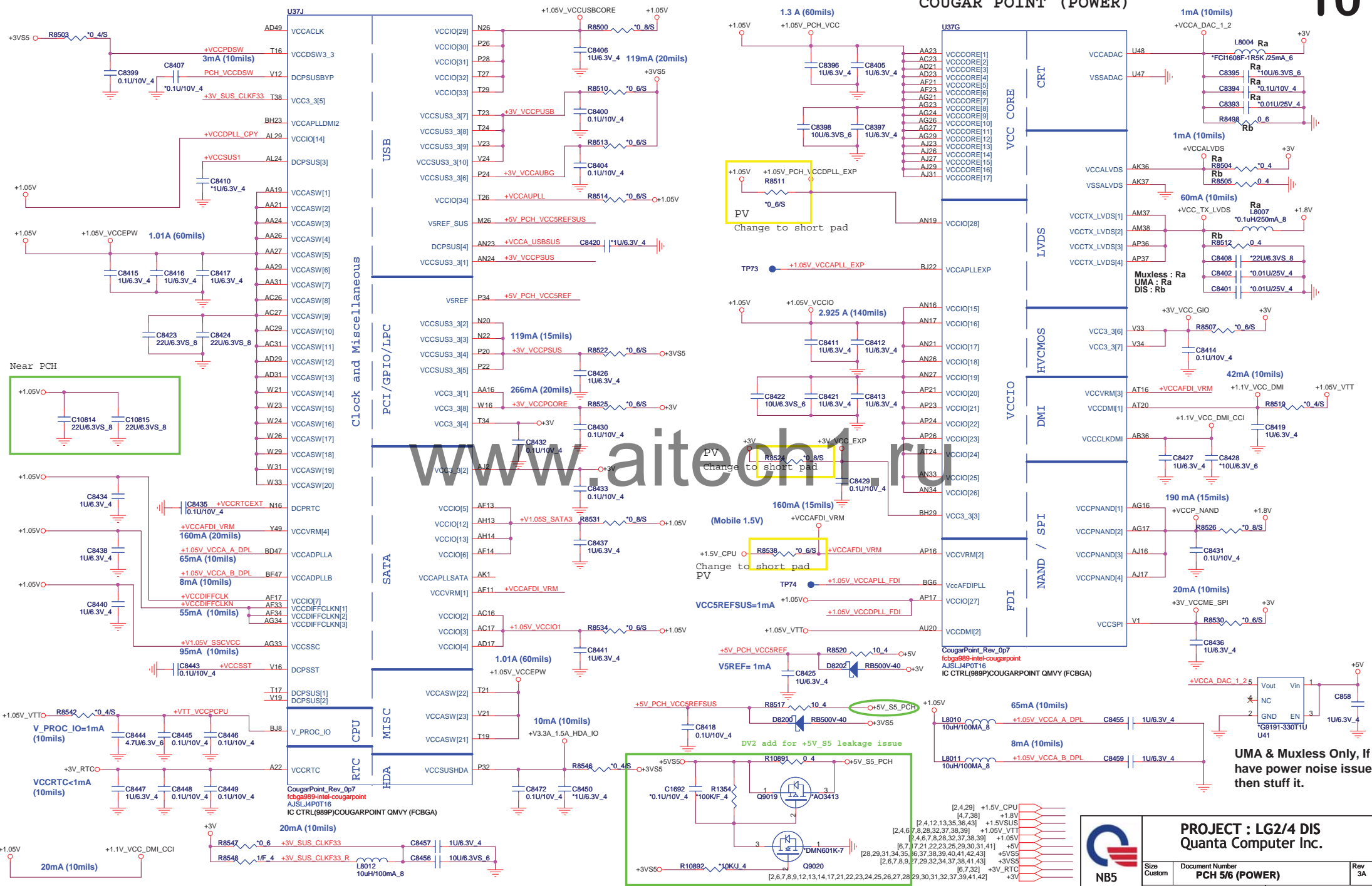
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 3A
Date: Wednesday, May 18, 2011	Sheet 9	of 47

Cougar Point-M (POWER)

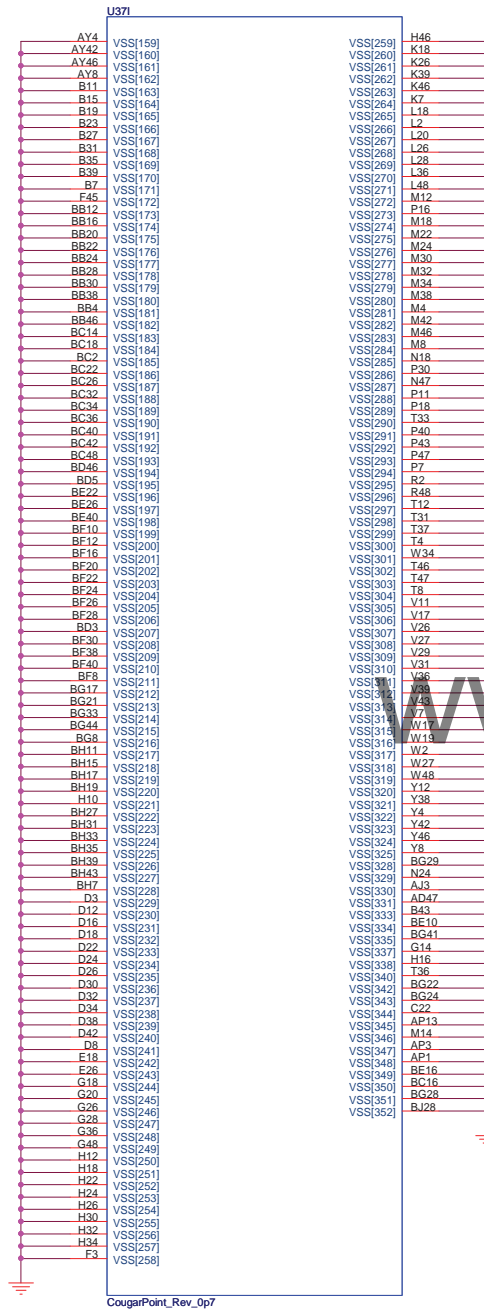
COUGAR POINT (POWER)

10

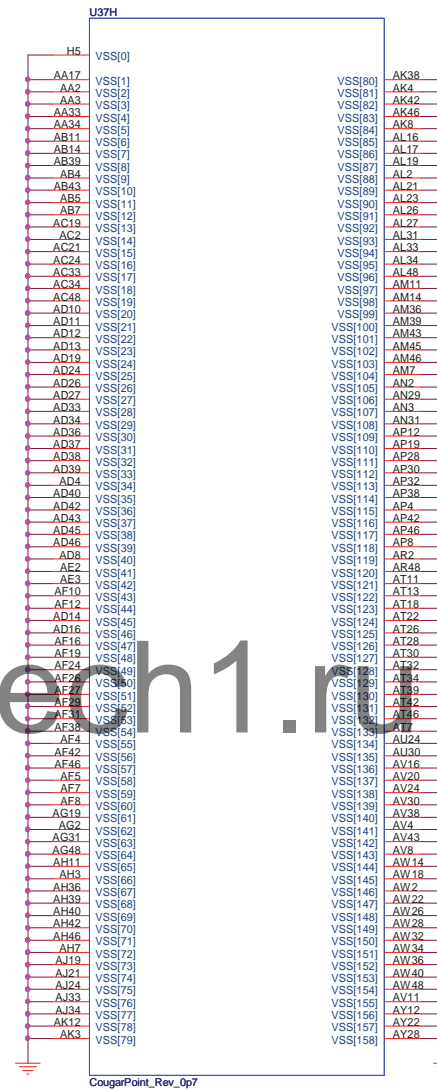


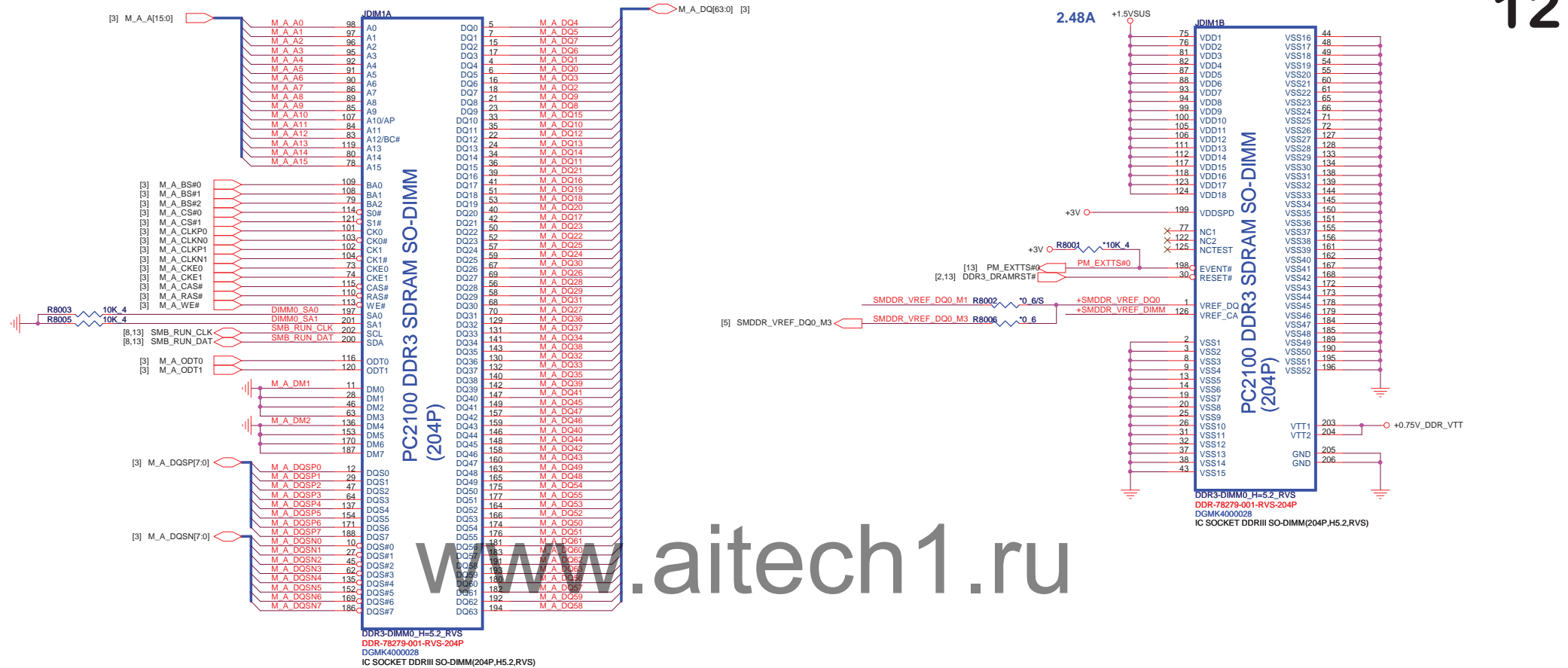
UMA & Muxless Only, If have power noise issue then stuff it.

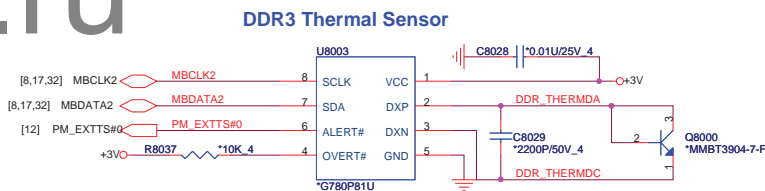
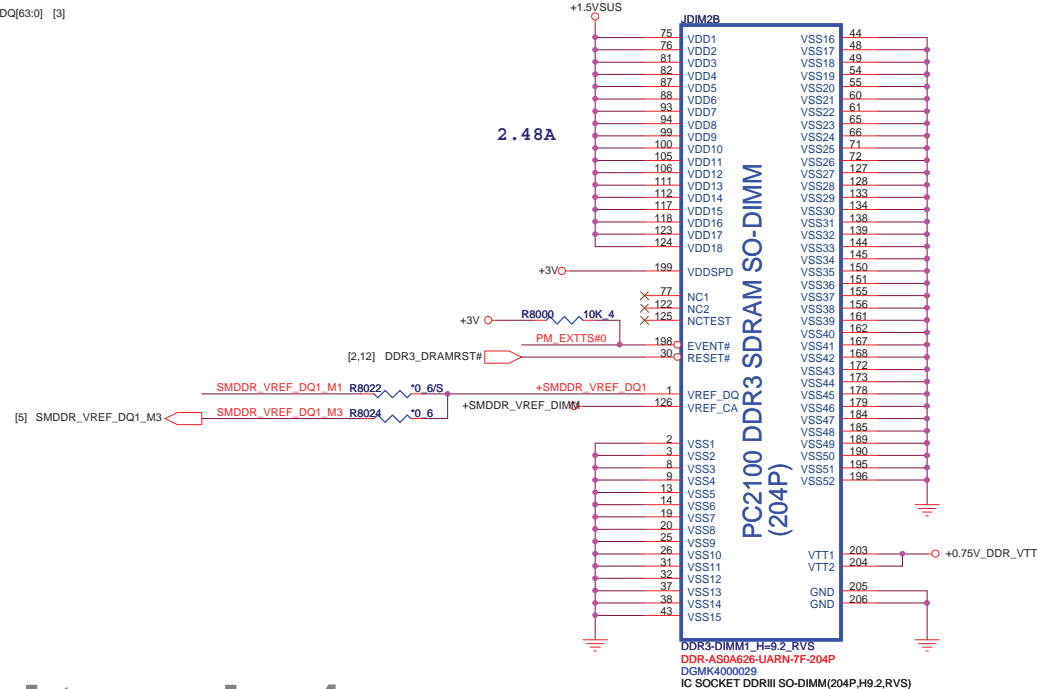
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)

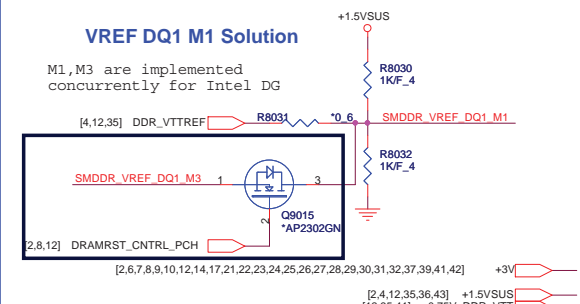






VREF DQ1 M1 Solution

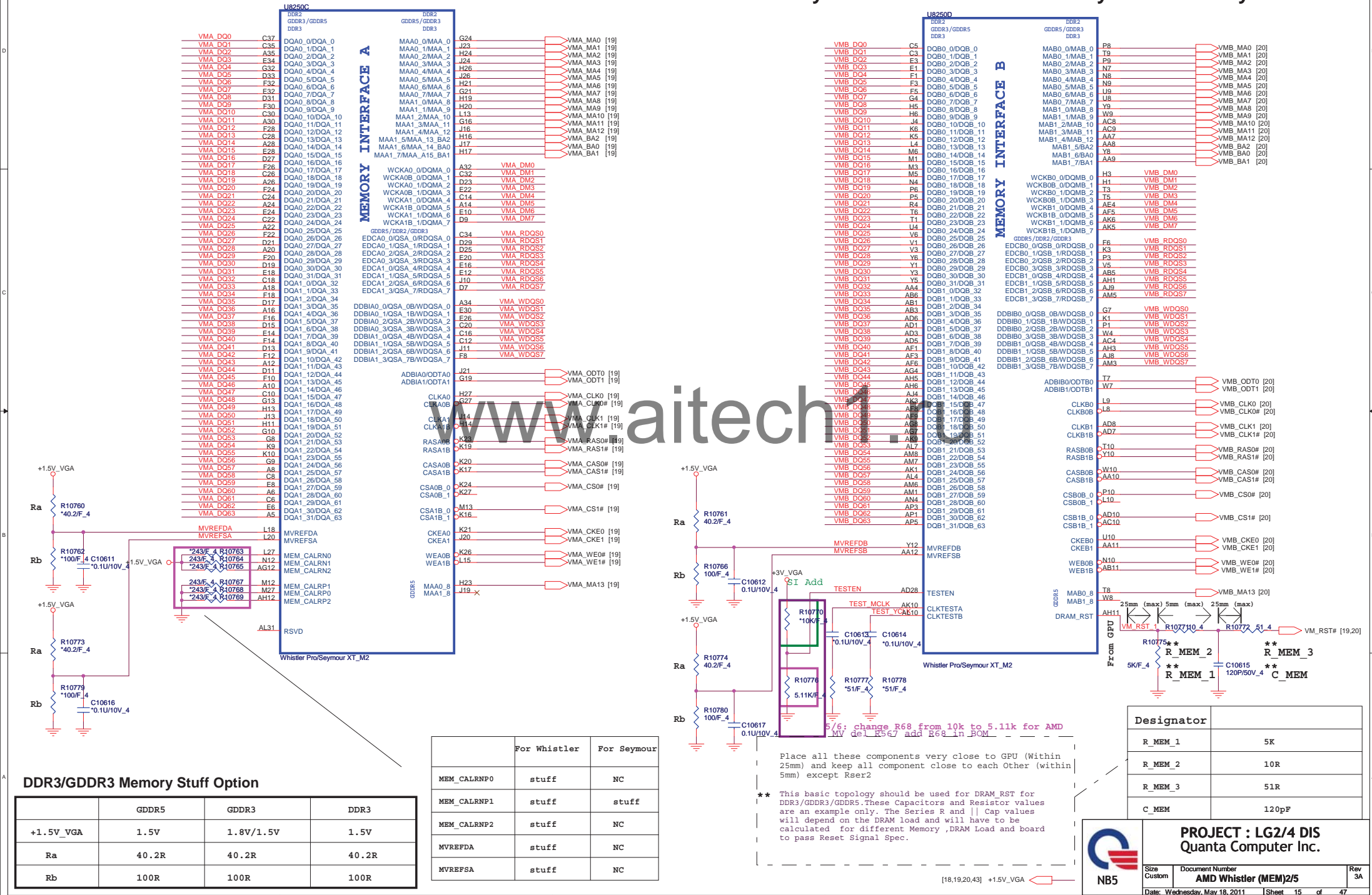
M1,M3 are implemented
concurrently for Intel DG



PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 3A
Date: Wednesday, May 18, 2011		Sheet 13 of 47

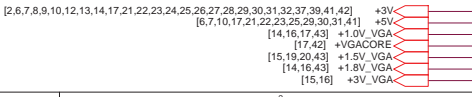
Seymour Use Channel B Memory Interface Only

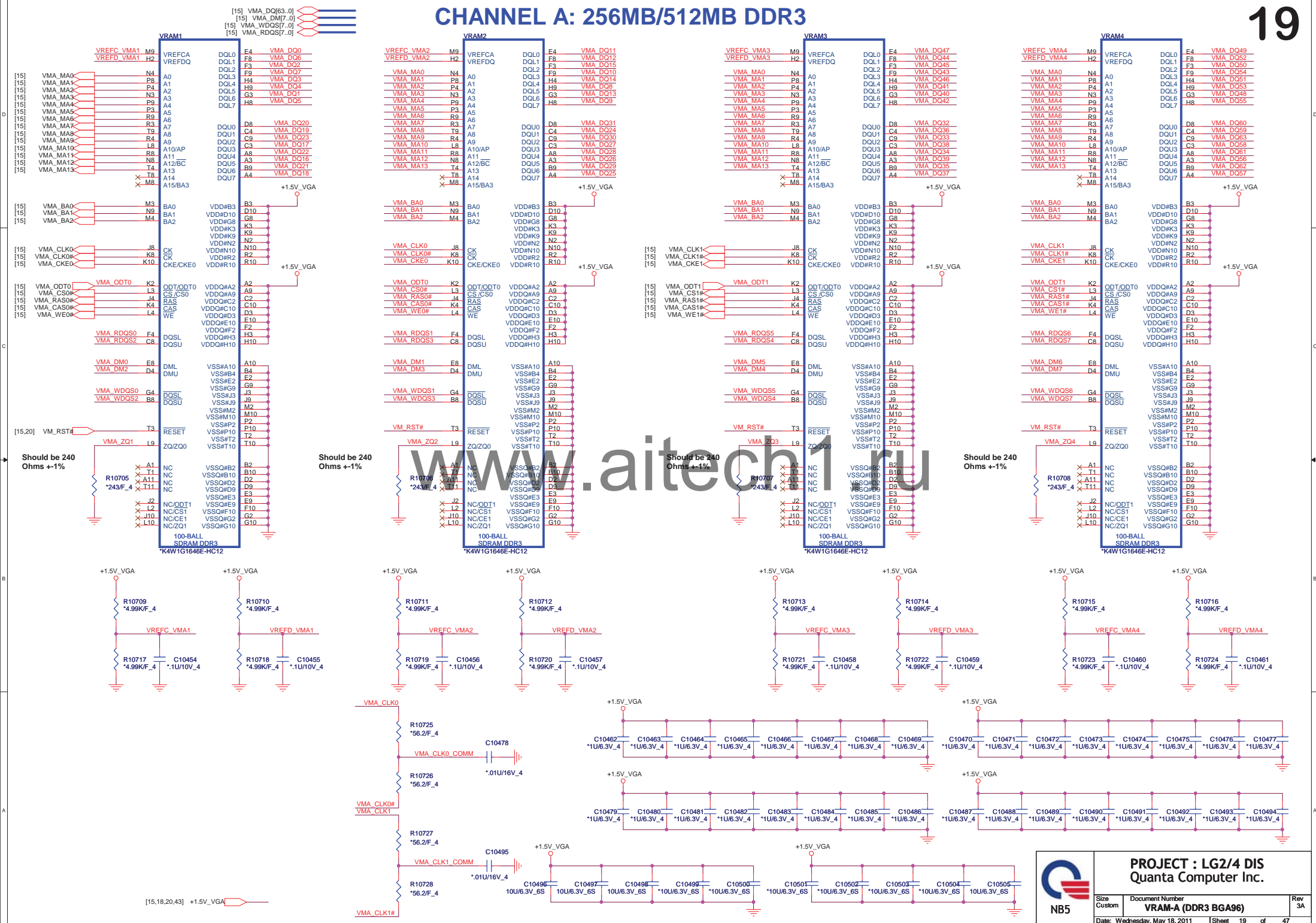


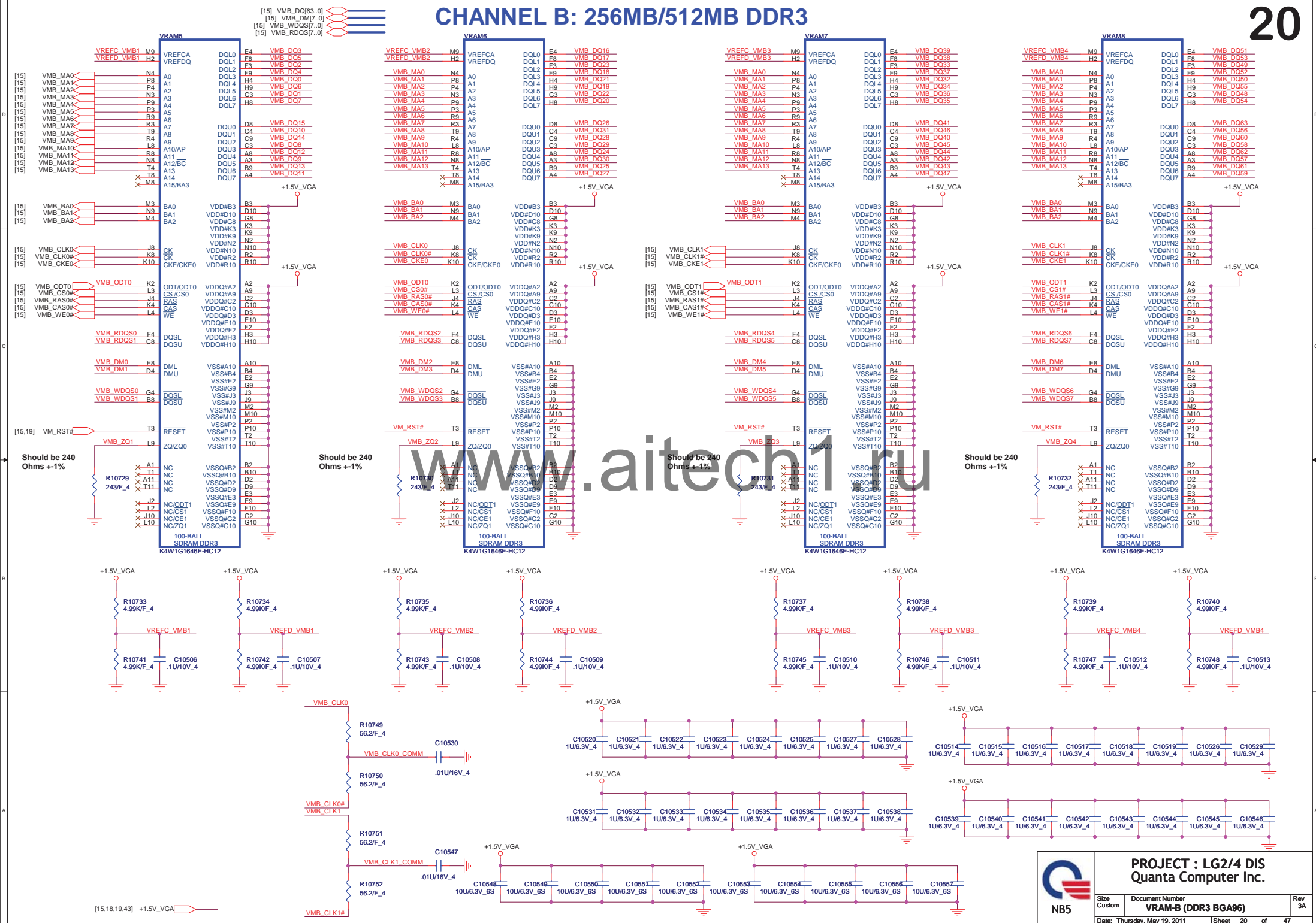


serve for support BACO mode









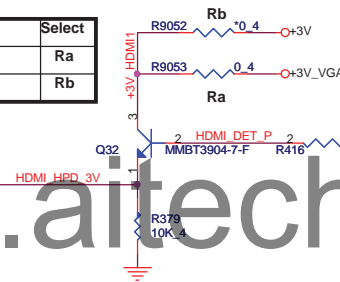
For DIS HDMI Only

[16]	N_TX2_HDMI+	C260	0.1U/10V_4	C_TX2_HDMI+	
[16]	N_TX2_HDMI-	C259	0.1U/10V_4	C_TX2_HDMI-	
[16]	N_TX1_HDMI+	C258	0.1U/10V_4	C_TX1_HDMI+	
[16]	N_TX1_HDMI-	C257	0.1U/10V_4	C_TX1_HDMI-	
[16]	N_TX0_HDMI+	C253	0.1U/10V_4	C_TX0_HDMI+	
[16]	N_TX0_HDMI-	C252	0.1U/10V_4	C_TX0_HDMI-	
[16]	N_TXC_HDMI+	C251	0.1U/10V_4	C_TXC_HDMI+	
[16]	N_TXC_HDMI-	C250	0.1U/10V_4	C_TXC_HDMI-	
[16]	HDMI_SDA	HDMI_SDA	R2	0.4	HDMI_SDA_R
[16]	HDMI_SCL	HDMI_SCL	R3	0.4	HDMI_SCL_R
[16]	TMDS_HPD	TMDS_HPD	R9025	0.4	HDMI_HPD_3V

Dis	Select
muxless	Ra

Ra

Dis	Select
Muxless	Ra

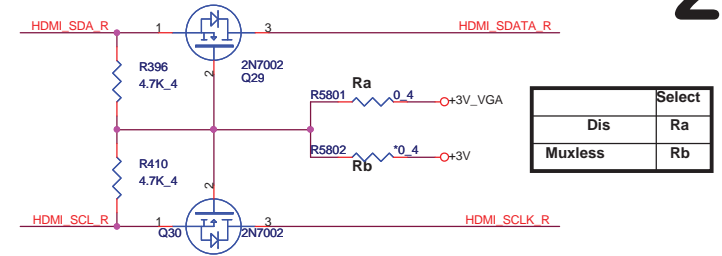


Dis	Select
Muxless	Rb

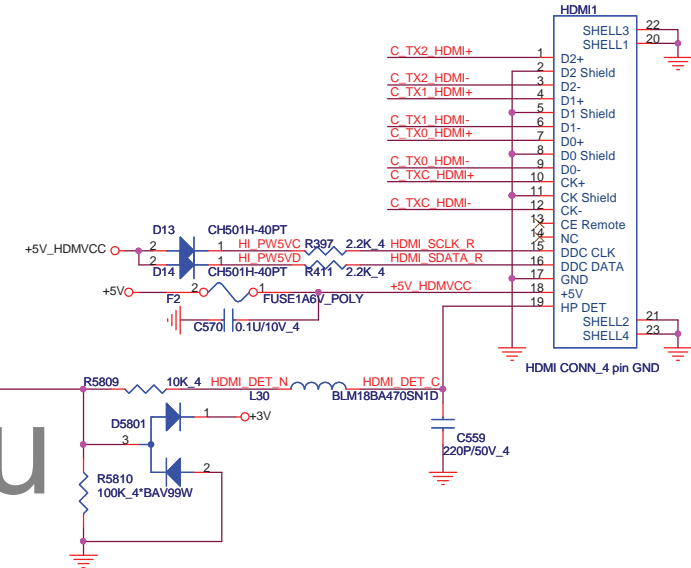
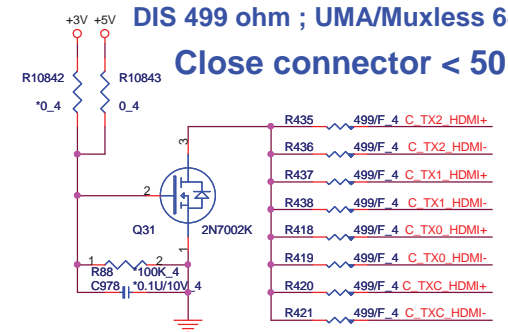
Rb

For Muxless/UMA HDMI function

[6]	IN_CLK#	C9027	*0.1U/10V_4	C_TXC HDMI-	
[6]	IN_CLK	C9028	*0.1U/10V_4	C_TXC HDMI+	
[6]	IN_D0#	C9029	*0.1U/10V_4	C_TX0 HDMI-	
[6]	IN_D0	C9030	*0.1U/10V_4	C_TX0 HDMI+	
[6]	IN_D1#	C9031	*0.1U/10V_4	C_TX1 HDMI-	
[6]	IN_D1	C9032	*0.1U/10V_4	C_TX1 HDMI+	
[6]	IN_D2#	C9033	*0.1U/10V_4	C_TX2 HDMI-	
[6]	IN_D2	C9034	*0.1U/10V_4	C_TX2 HDMI+	
[6]	SDVO_DATA	SDVO_DATA	R9035	*0.4	HDMI_SDA_R
[6]	SDVO_CLK	SDVO_CLK	R9036	*0.4	HDMI_SCL_R
[6]	HDMI_HPD_CON	HDMI_HPD_CON	R9021	*0.4	HDMI_HPD_3V

DIS: 4.7K
UMA/Muxless: 2.2K

Dis	Select
Muxless	Rb

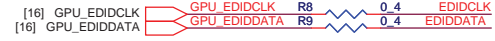
DIS 499 ohm ; UMA/Muxless 680 ohm
Close connector < 50 mil

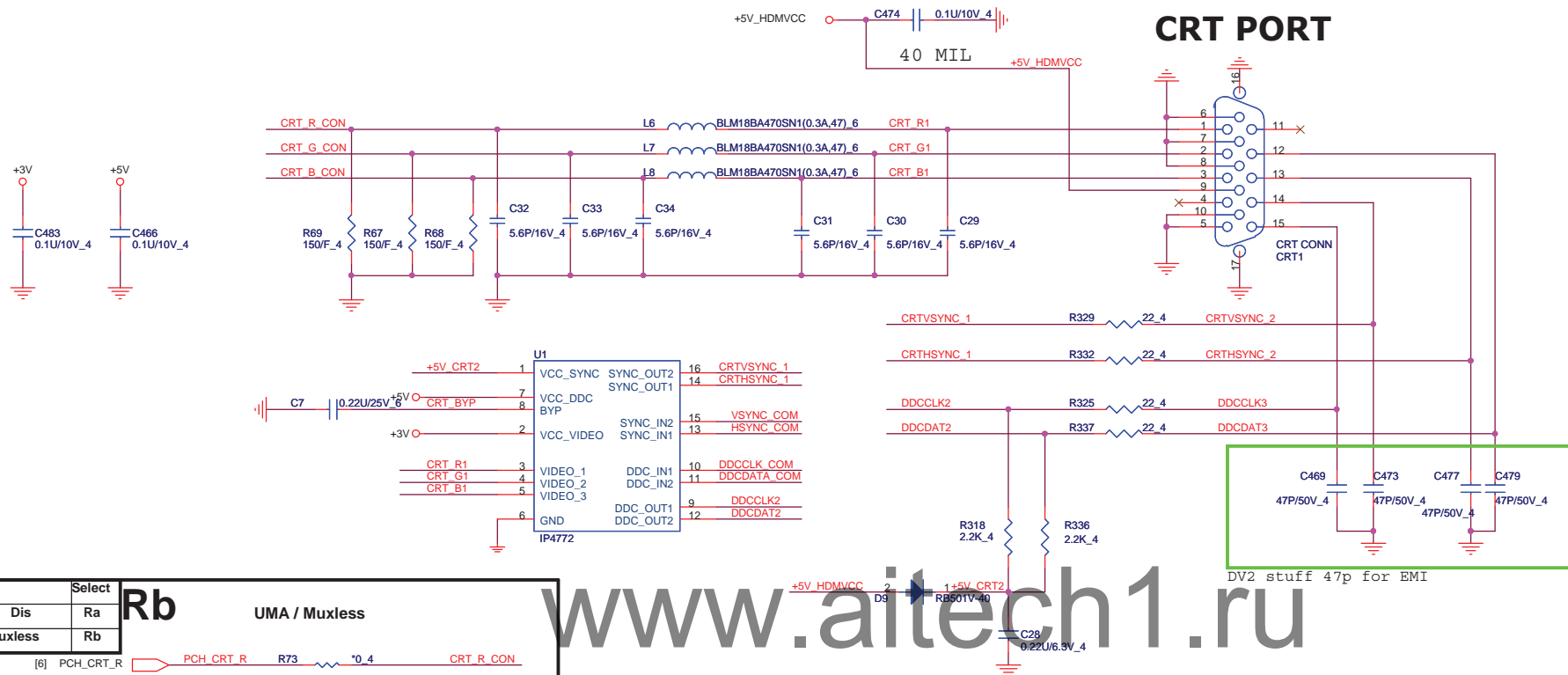
Close connector < 50 mil

C_TXC_HDMI+	R135	150/F_4	C_TXC_HDMI-
C_TX0_HDMI+	R136	150/F_4	C_TX0_HDMI-
C_TX1_HDMI+	R141	150/F_4	C_TX1_HDMI-
C_TX2_HDMI+	R142	150/F_4	C_TX2_HDMI-















DV2 Change to 150 ohm


	PROJECT : LG2/4 DIS Quanta Computer Inc.		Rev 3A	
	Size Custom	Document Number HDMI and connector		
	Date: Friday, May 20, 2011	Sheet 21 of 47		





Select		Rb	UMA / Muxless
Dis	Ra		
muxless		Rb	

[6]	PCH_CRT_R		PCH_CRT_R	R73		*0_4	CRT_R_CON
[6]	PCH_CRT_G		PCH_CRT_G	R74		*0_4	CRT_G_CON
[6]	PCH_CRT_B		PCH_CRT_B	R75		*0_4	CRT_B_CON
[6]	PCH_HSYNC		PCH_HSYNC	R17		*0_4	HSYNC_CON
[6]	PCH_VSYNC		PCH_VSYNC	R23		*0_4	VSYNC_CON
[6]	PCH_DDCCLK		PCH_DDCCLK	R24		*0_4	DDCCLK_CON
[6]	PCH_DDCDATA		PCH_DDCDATA	R16		*0_4	DDCDATA_CON



DIS Only

[16]	GPU_CRT_R	GPU_CRT_R	R70	0.4	CRT_R_CON
[16]	GPU_CRT_G	GPU_CRT_G	R71	0.4	CRT_G_CON
[16]	GPU_CRT_B	GPU_CRT_B	R72	0.4	CRT_B_CON
[16,17]	GPU_HSYNC	GPU_HSYNC	R20	0.4	HSYNC_CON
[16,17]	GPU_VSYNC	GPU_VSYNC	R15	0.4	VSYNC_CON
[16]	GPU_DDCCLK	GPU_DDCCLK	R21	0.4	DDCCLK_CON
[16]	GPU_DDCDATA	GPU_DDCDATA	R18	0.4	DDCDATA_CON

DIS Only / Muxless stuff

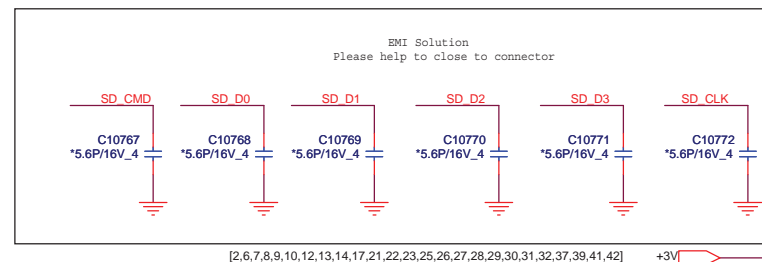
+3V_VGA

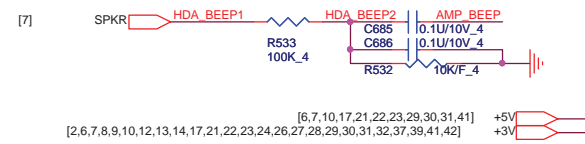
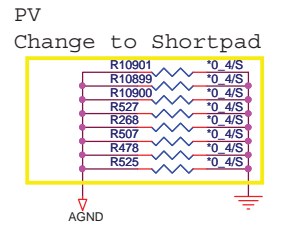
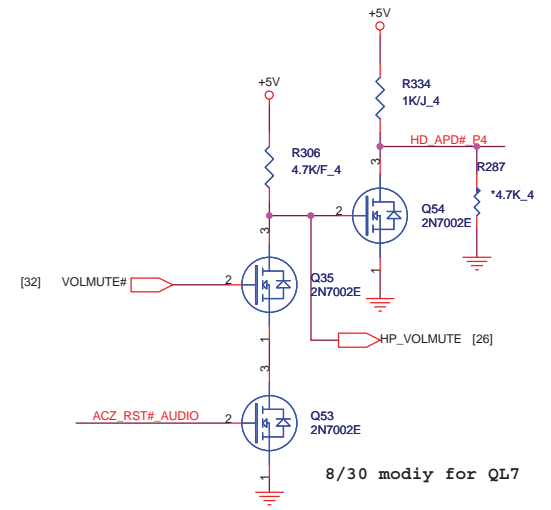
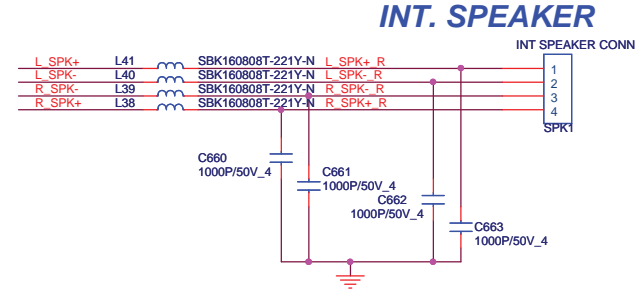
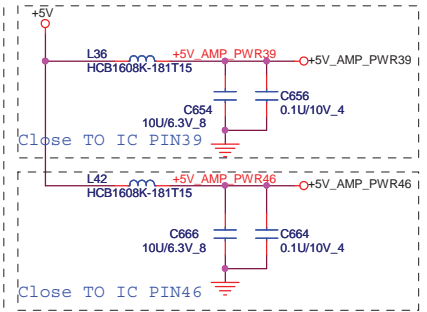
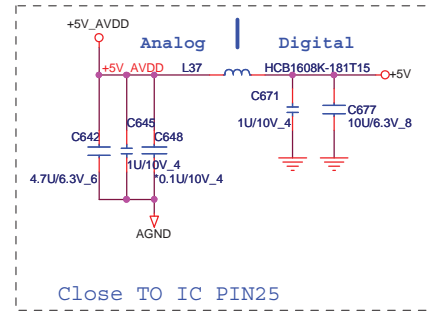
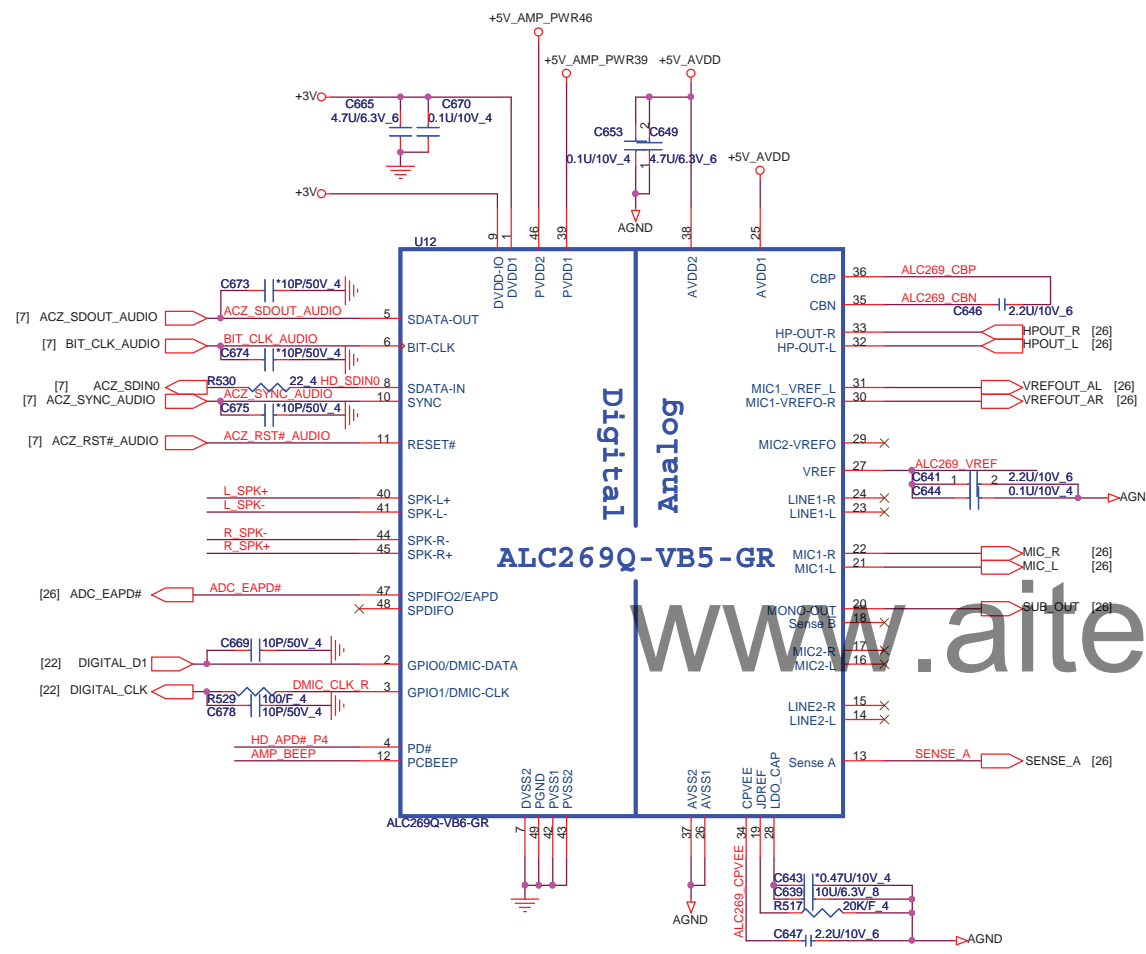
R313 4.7K/4 GPU DDCLK

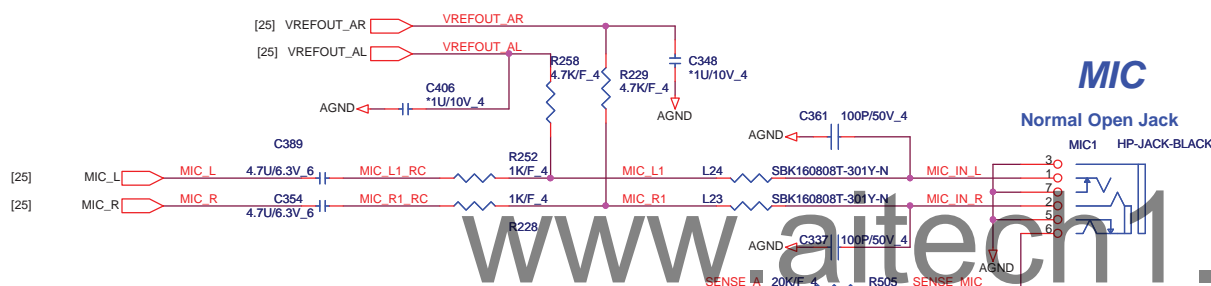
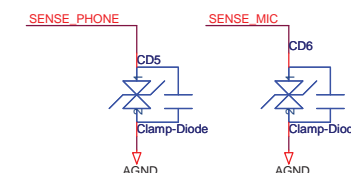
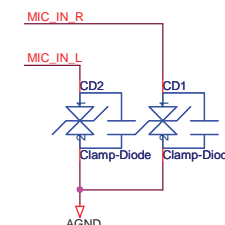
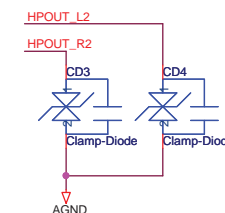
R316 4.7K/4 GPU DDCDATA

AV12 R6 0 4 DV12

Reserved

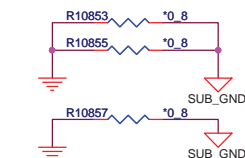
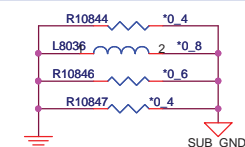






The schematic shows the U8252 component with the following connections:

- Pin 1 (SD):** Connected to ADC_EAPD# via R10845 (*100K 4).
- Pin 2 (FAULT):** Connected to +3V via R10848 (*100K 4).
- Pin 3 (NC_3):** Not connected.
- Pin 4 (NC_4):** Not connected.
- Pin 5 (GAIN0):** Connected to SUB_GND via R10851 (*0.6/S).
- Pin 6 (GAIN1):** Connected to SUB_GND via R10854 (*0.6/S).
- Pin 7 (AVCC):** Connected to PVCC2 via R10856 (*10.6) and C10735 (*1U/25V 6).
- Pin 8 (AGND):** Connected to SUB_GND via C10737 (*1U/25V 6) and R10858 (*47.5K/F 6).
- Pin 9 (GVDD):** Connected to SUB_GND via C10738 (*1U/25V 6) and R10859 (*27.4K/F 6).
- Pin 10 (PLIMIT):** Not connected.
- Pin 11 (INN):** Connected to SUB_GND via C10741 (*1U/25V 6) and R8034 (*0.6).
- Pin 12 (INP):** Connected to SUB_OUT via C10742 (*1U/25V 6) and R8036 (*0.6).
- Pin 13 (NC_13):** Not connected.
- Pin 14 (AVCC):** Connected to PVCC2 via R10860 (*10K 6).
- Pin 15 (PVCC):** Connected to PVCC2 via C10745 (*0.1U/50V 6).
- Pin 16 (PVCC):** Connected to PVCC2 via C10744 (*1000P/50V 6).
- Pin 17 (BSP_17):** Connected to PVCC2 via C10743 (*0.22U/50V 8).
- Pin 18 (OUTP_18):** Connected to SUB_GND via C10736 (*0.22U/50V 8).
- Pin 19 (PGND):** Connected to SUB_GND via C10733 (*0.22U/50V 8).
- Pin 20 (OUTP_20):** Connected to SUB_GND via C10734 (*0.22U/50V 8).
- Pin 21 (BSP_21):** Connected to SUB_GND via C10732 (*0.1U/50V 6).
- Pin 22 (BSN_22):** Connected to SUB_GND via C10731 (*1000P/50V 6).
- Pin 23 (OUTN_23):** Connected to SUB_GND via C10730 (*1000P/50V 6).
- Pin 24 (PGND):** Connected to SUB_GND via C10733 (*0.22U/50V 8).
- Pin 25 (OUTN_25):** Connected to SUB_GND via C10733 (*0.22U/50V 8).
- Pin 26 (BSN_26):** Connected to SUB_GND via C10733 (*0.22U/50V 8).
- Pin 27 (PVCC):** Connected to PVCC2 via C10732 (*0.1U/50V 6).
- Pin 28 (PVCC):** Connected to PVCC2 via C10730 (*1000P/50V 6).



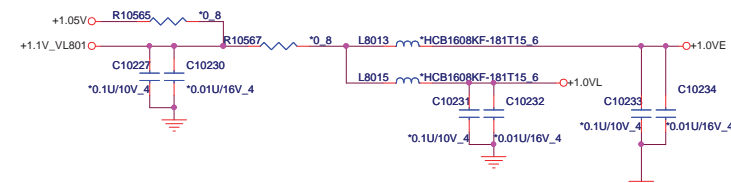
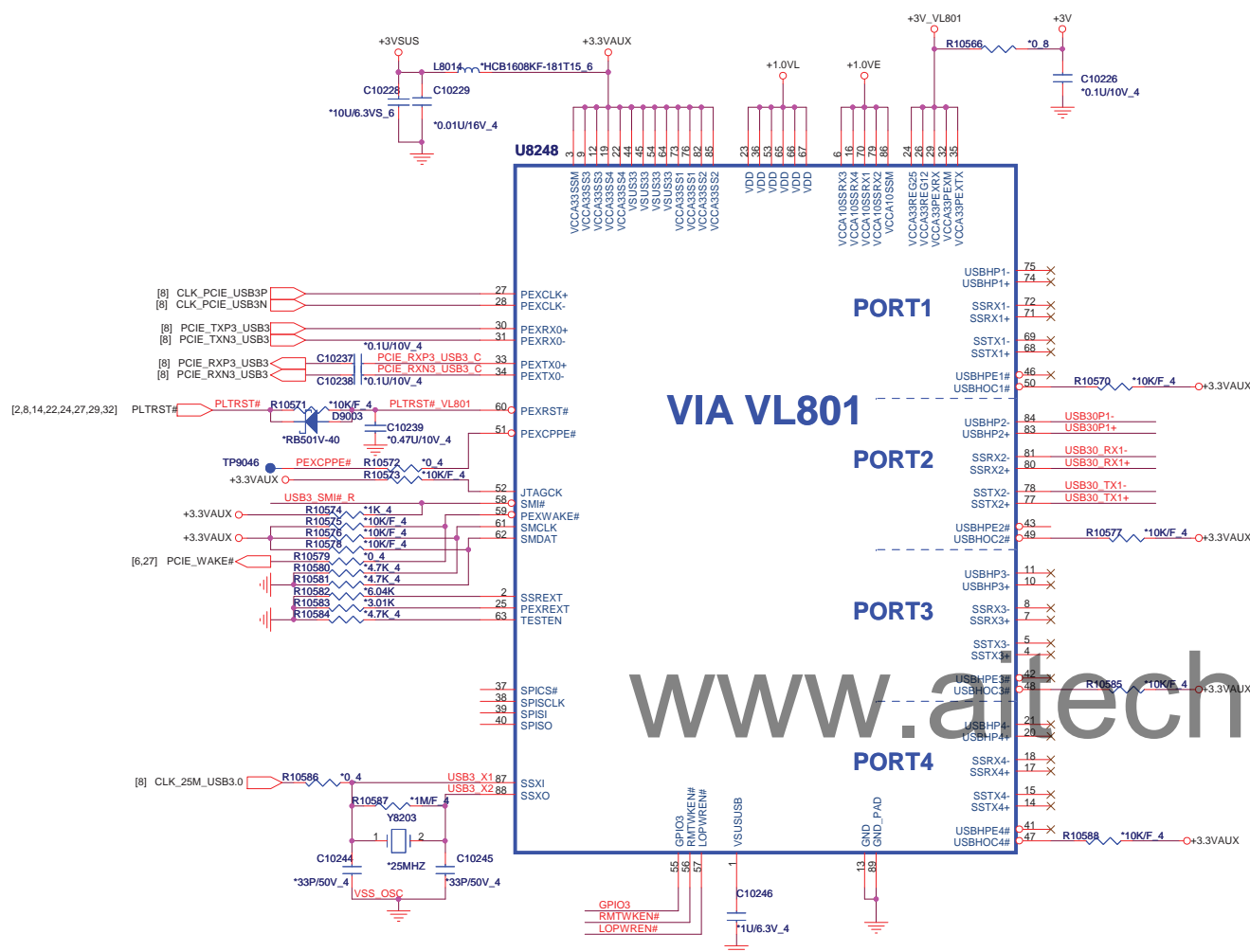
GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36

[22,29,33,34,35,36,37,40,41,42,43] +VIN
[6,7,10,17,21,22,23,25,29,30,31,41] +5V
[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,27,28,29,30,31,32,37,39,41,42] +3V



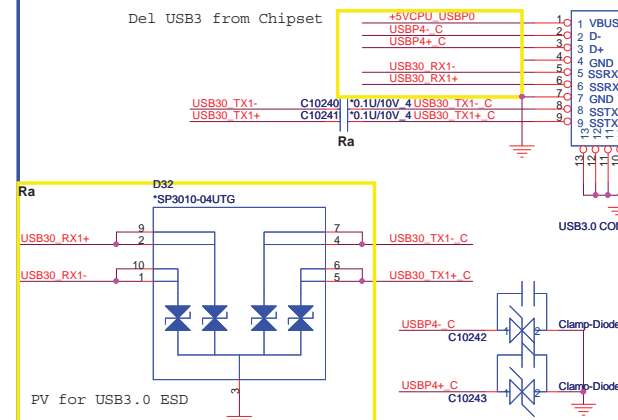
PROJECT : LG2/4 DIS
Quanta Computer Inc.

Size Custom	Document Number Audio Jack/Accelerometer	R
Date: Wednesday, May 18, 2011		Sheet 26 of 47



USB3.0/USB2.0 x1 COMBO

Del USB3 from Chipset



CTL1	CTL2	CTL3	TPS2540 Control Truth Table
0	0	0	Out Discharge ,Power switch OFF
0	X	1	Dedicated charging port, auto-detect (DCP)
X	1	0	Standard downstream port, USB 2.0 Mode.(SDP)
1	1	1	Charging downstream port, BC1.2 (draft).(CDP)

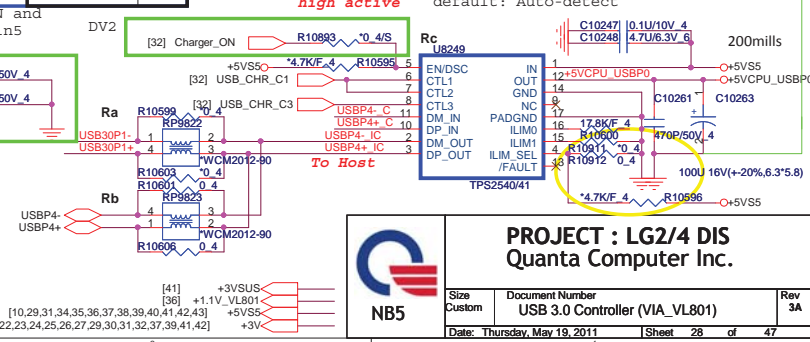
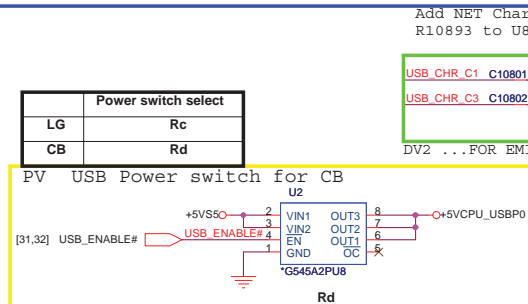
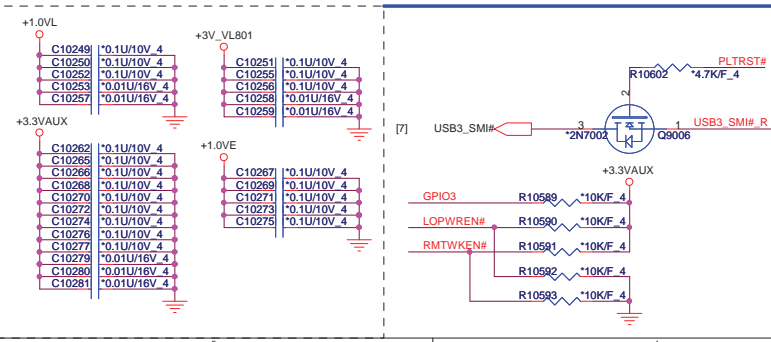
LGE SPEC	S0/S3		S4/S5	
	AC Mode	DC Mode	AC Mode	DC Mode
change mode	CDP	CDP	DCP	DCP
User define Battery % and wake up from USB		SDP		OFF

Charger USB

Add R10911,R10912,R10596 for TPS2543

80 mils (Iout=2A)

Ios = 48000/RILIM0
default: Auto-detect

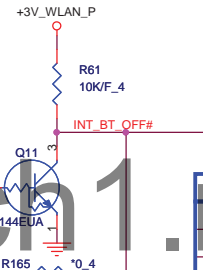
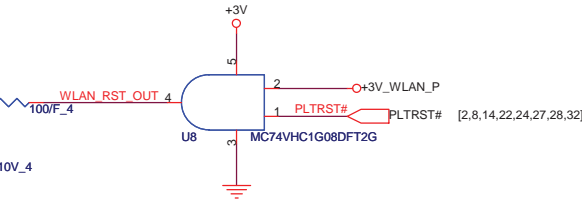
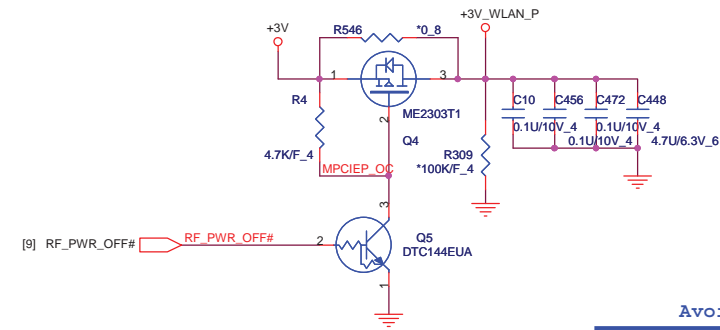
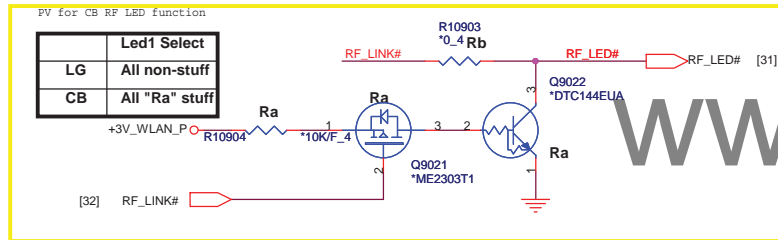
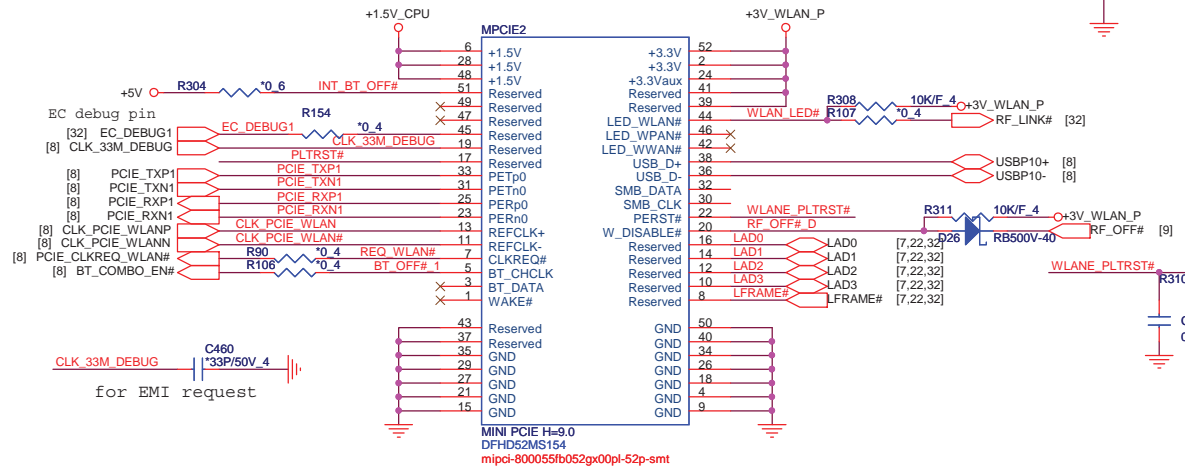


PROJECT : LG2/4 DIS
Quanta Computer Inc.

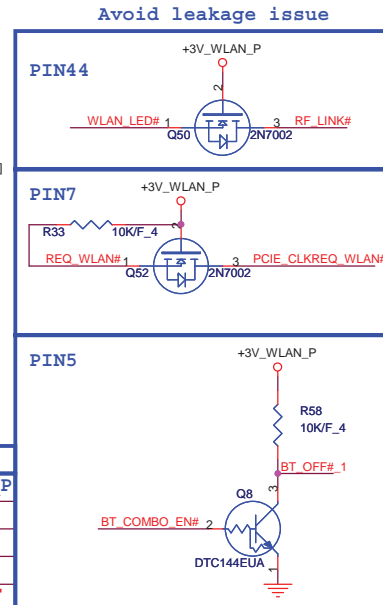


Size Custom	Document Number USB 3.0 Controller (VIA_VL801)	Rev 3A
Date: Thursday, May 19, 2011		Sheet 28 of 47

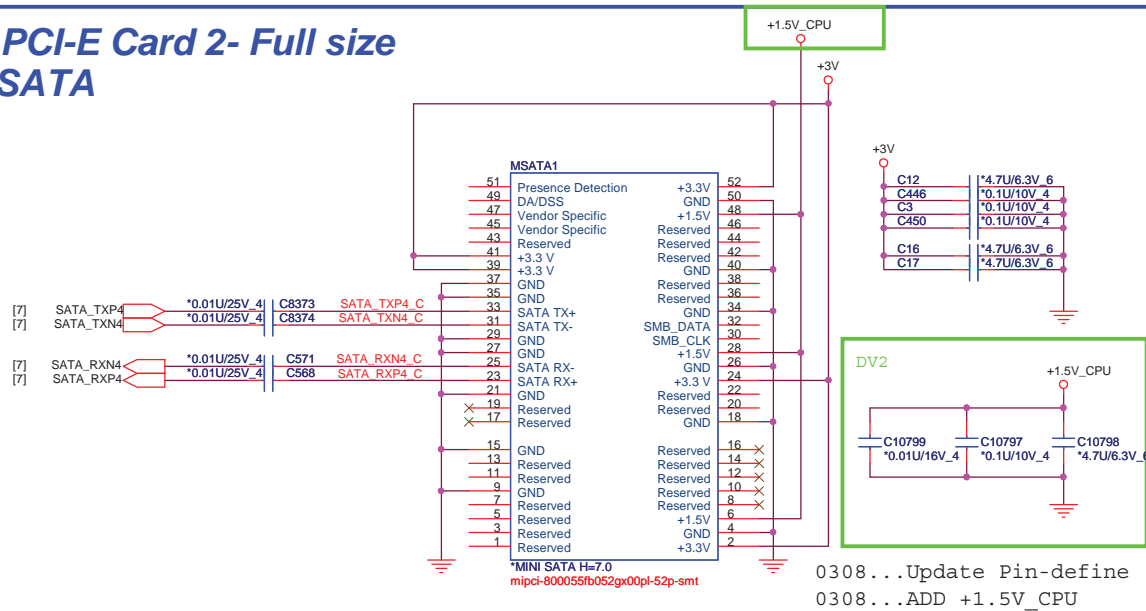
Mini PCI-E Card 1 - Half WLAN



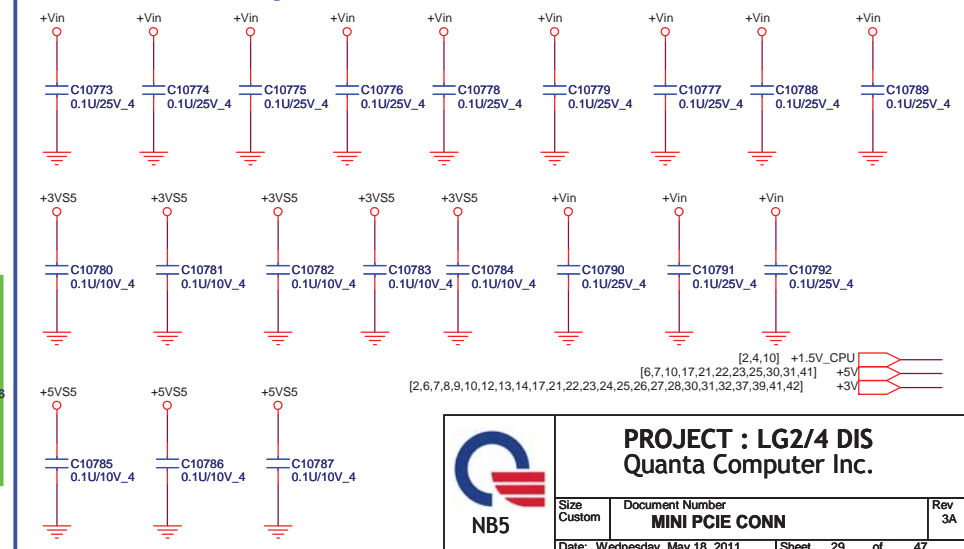
LGE mini-pcie power status		
WLAN	Bluetooth	+3V_WLAN_
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF



Mini PCI-E Card 2- Full size MINISATA

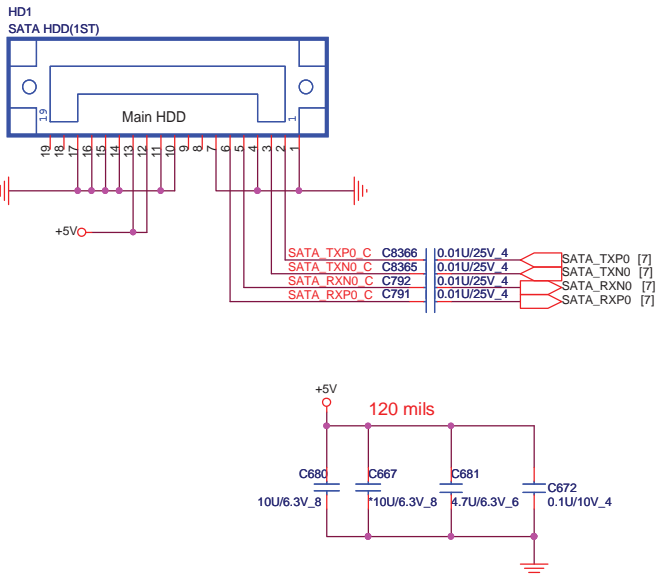


Power Plan Cap for EMI



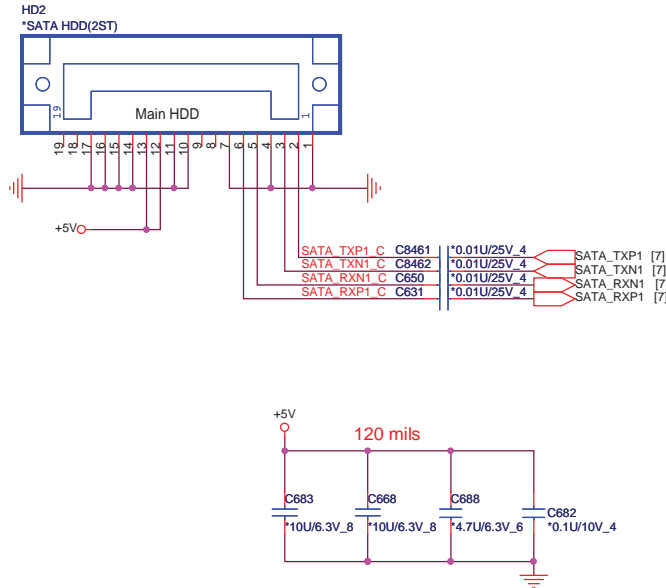
MAIN SATA HDD

DC Current rating: 0.5 A



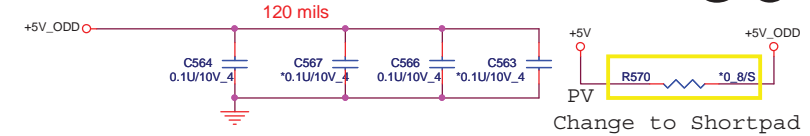
2nd SATA HDD for 17"

DC Current rating: 0.5 A



SATA CD-ROM To ODD Board

30

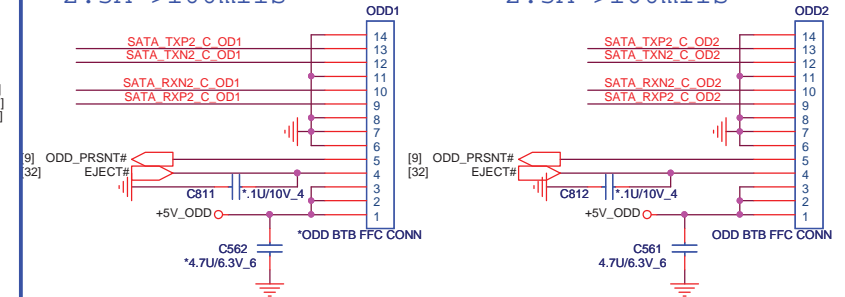


For 17" place

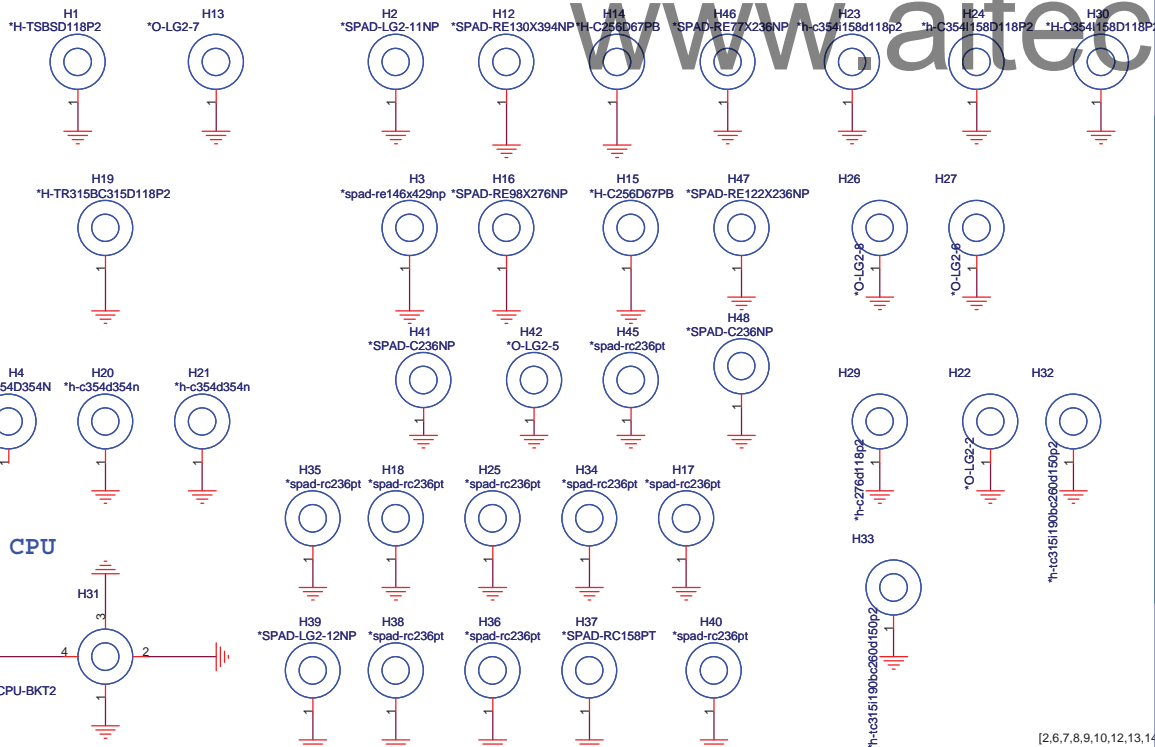
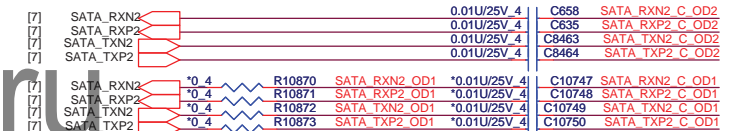
2.5A >100mils

For 14"/15" place

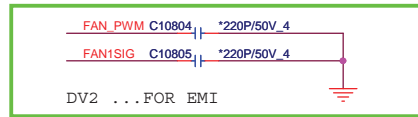
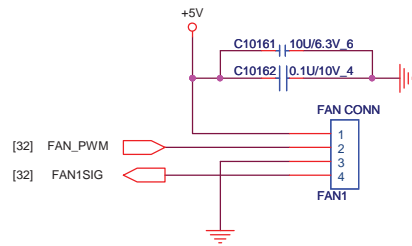
2.5A >100mils



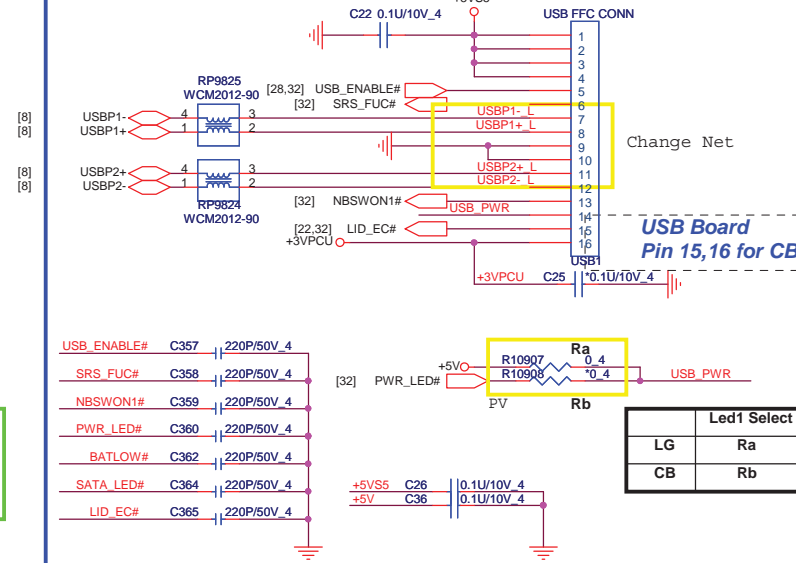
Ra FOR 14"/15"
Rb FOR 17"



CPU FAN



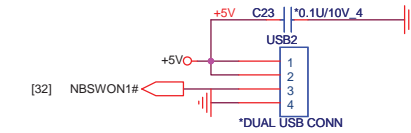
USB / Power LED & SW for 14"/15"/17" To USB Board



Change Net

USB Board Pin 15,16 for CB	
LG	Ra
CB	Rb

Power SW for 17"

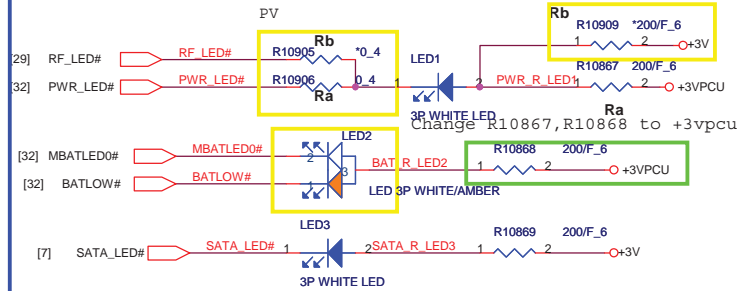


LED Select Pin

Led1 Select	
LG	Ra
CB	Rb

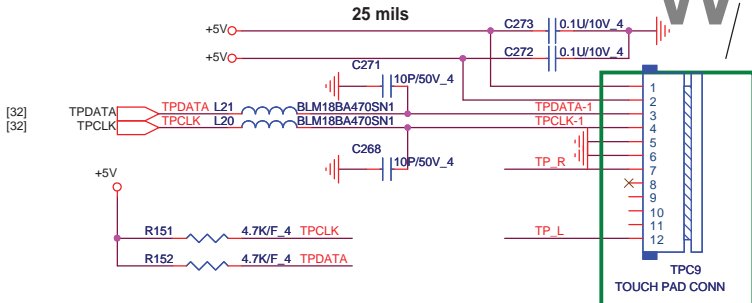
Led2 P/N	
LG	BEWH0051Z00
CB	BEWY0007ZA0

10 mils (250mA)

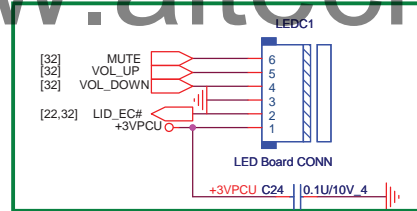


TOUCH PAD CONNECTOR To Click Board & FP

Update TPC9 footprint & P/N...0303

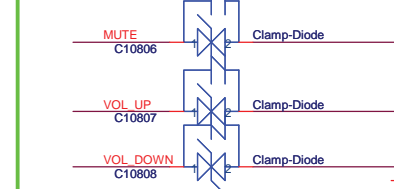


LID / MUTE / VU UP / VU DO To AD Function Board

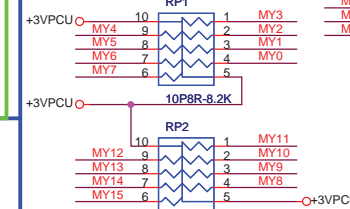


Update LEDC1 footprint & P/N...0303

DV2 ...FOR EMI



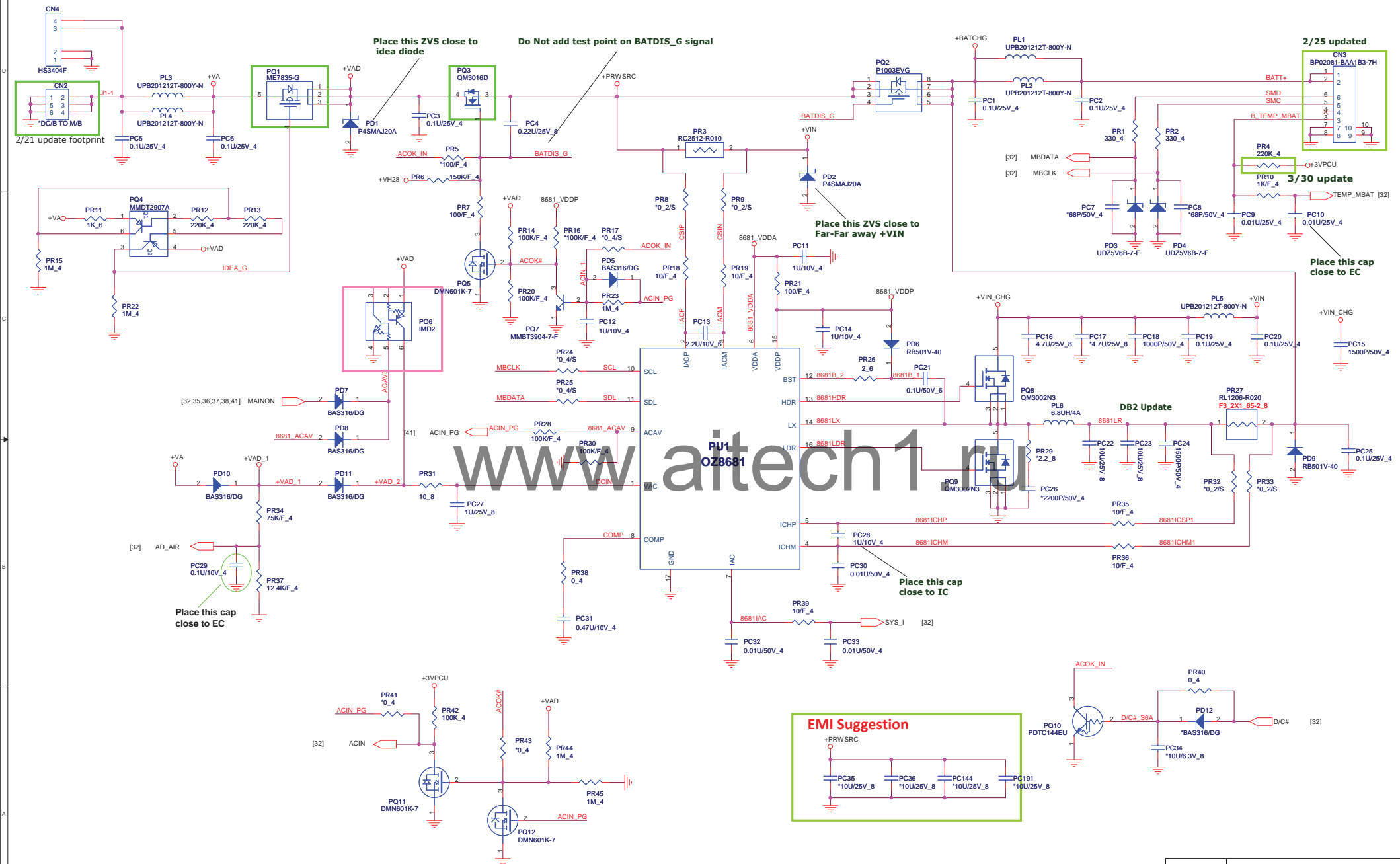
KEYBOARD PULL-UP

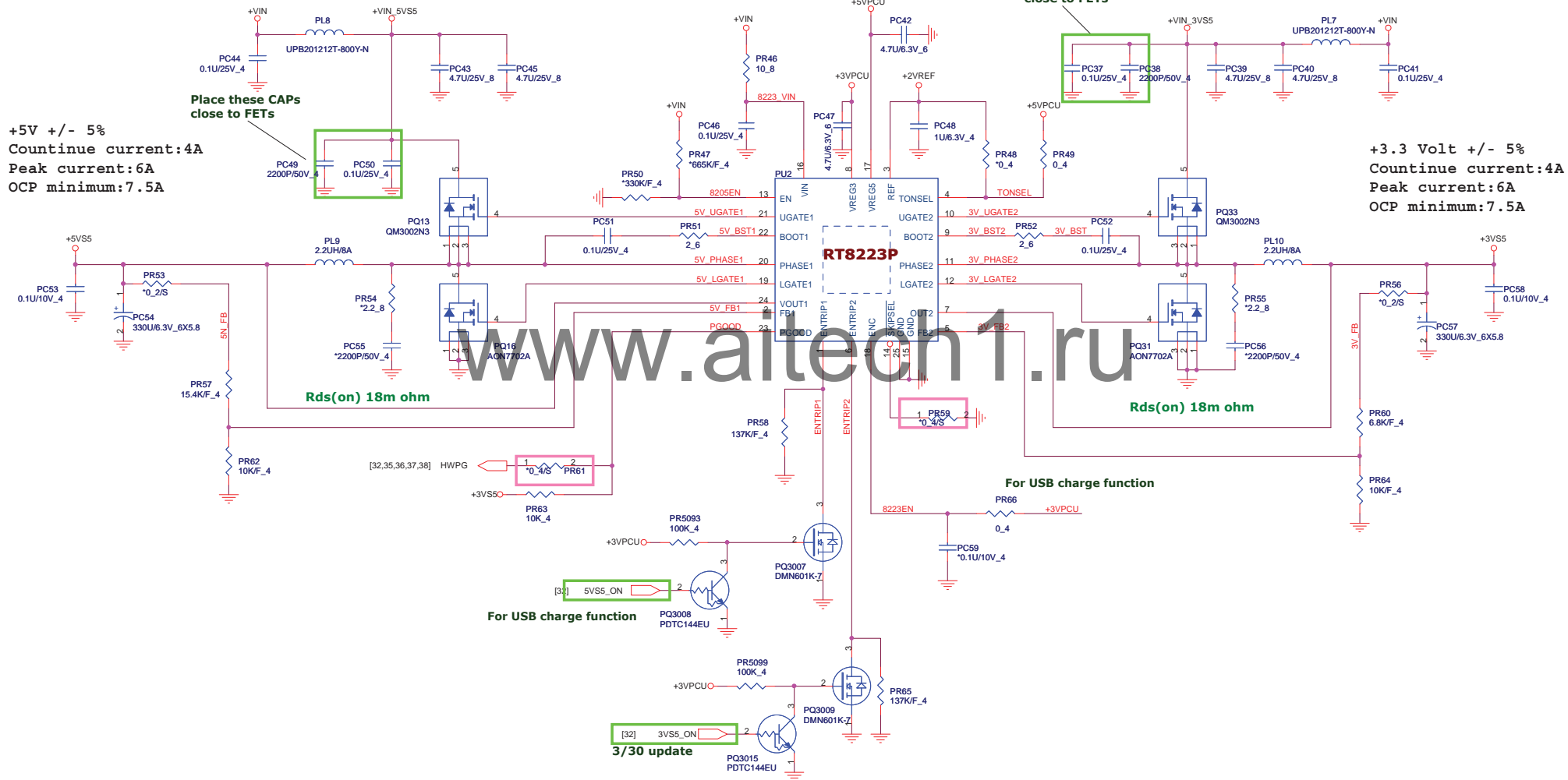


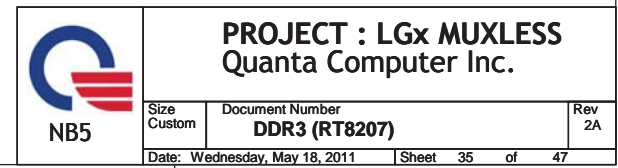


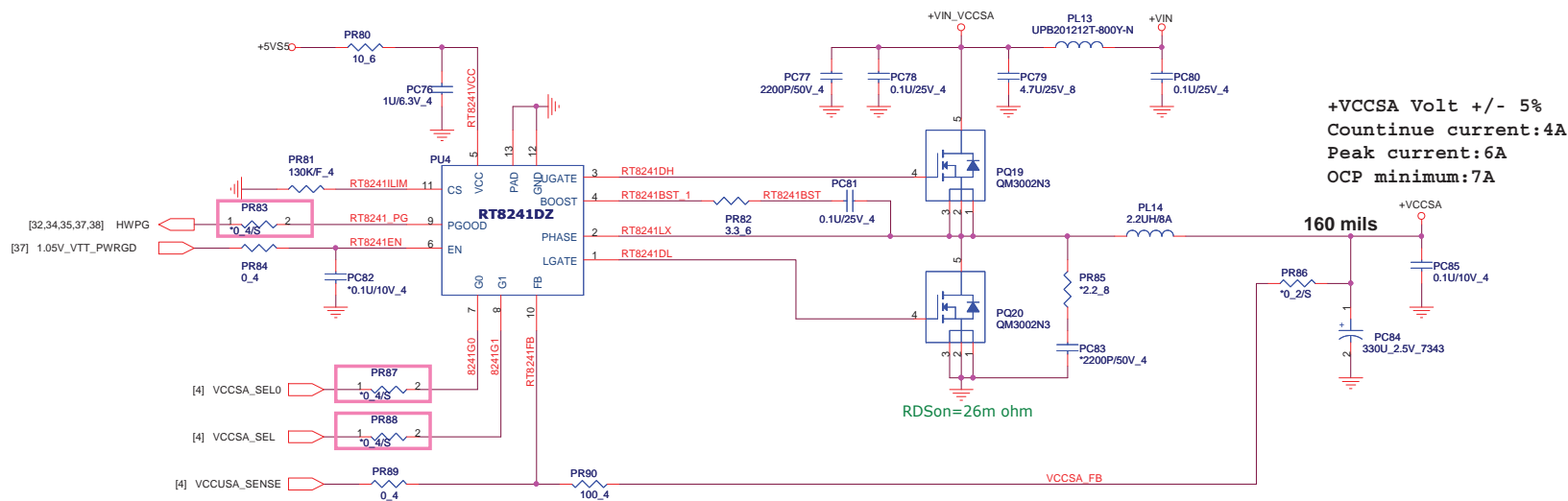
**TOP DC_JACK
90W/120W(QC)**

LG2_DIS only

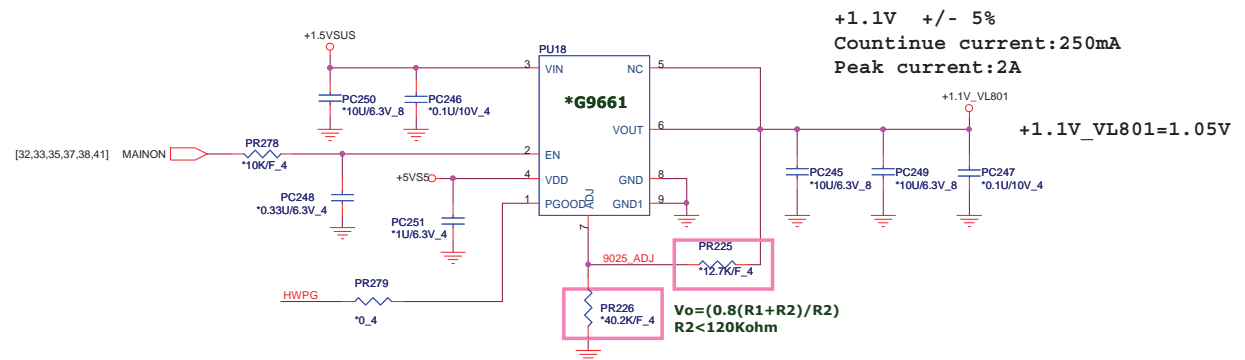


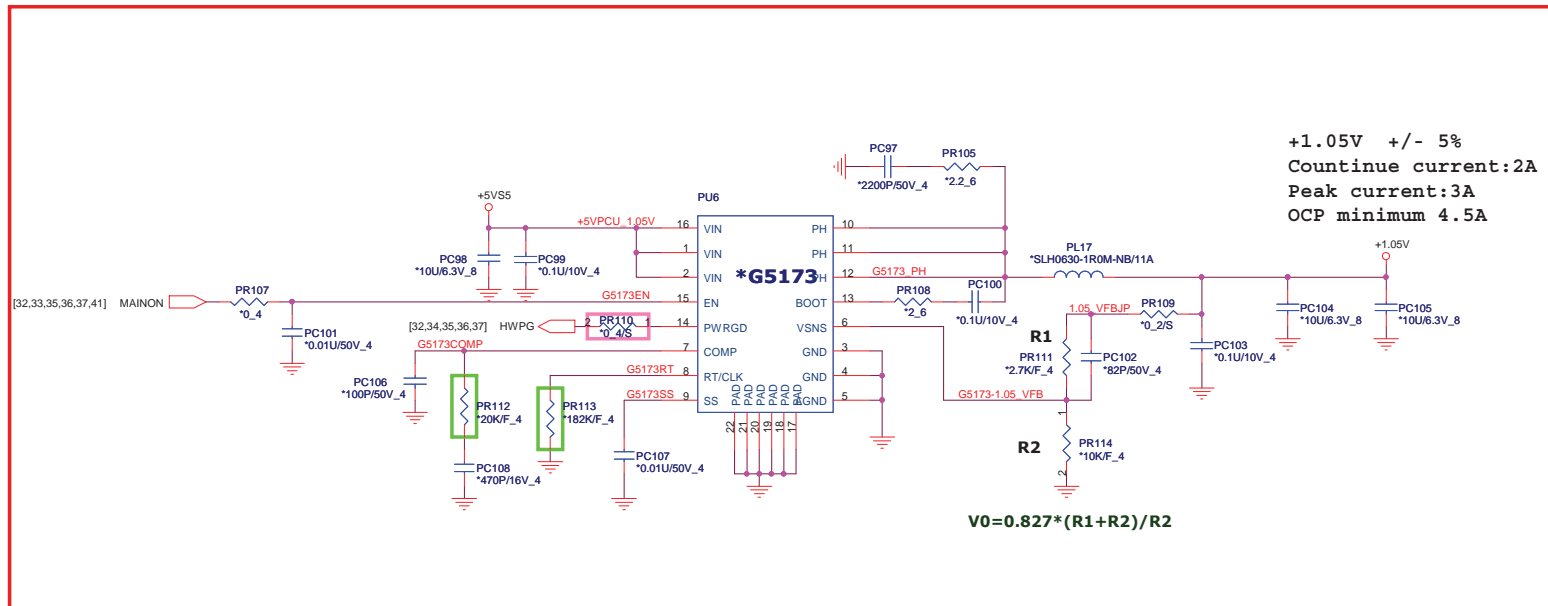




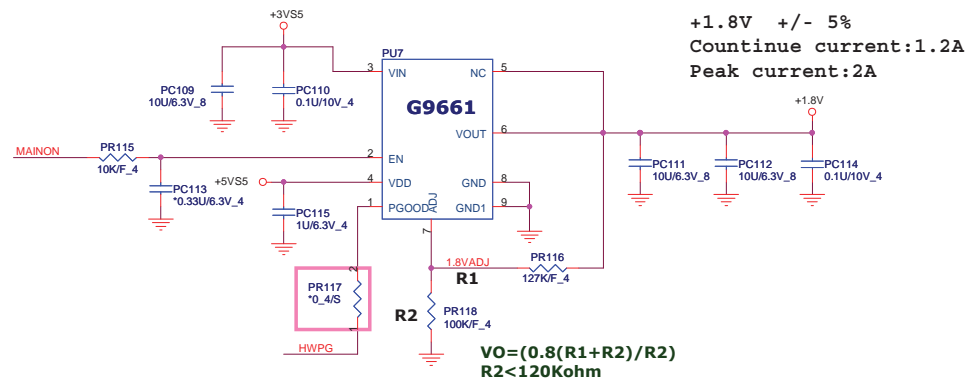


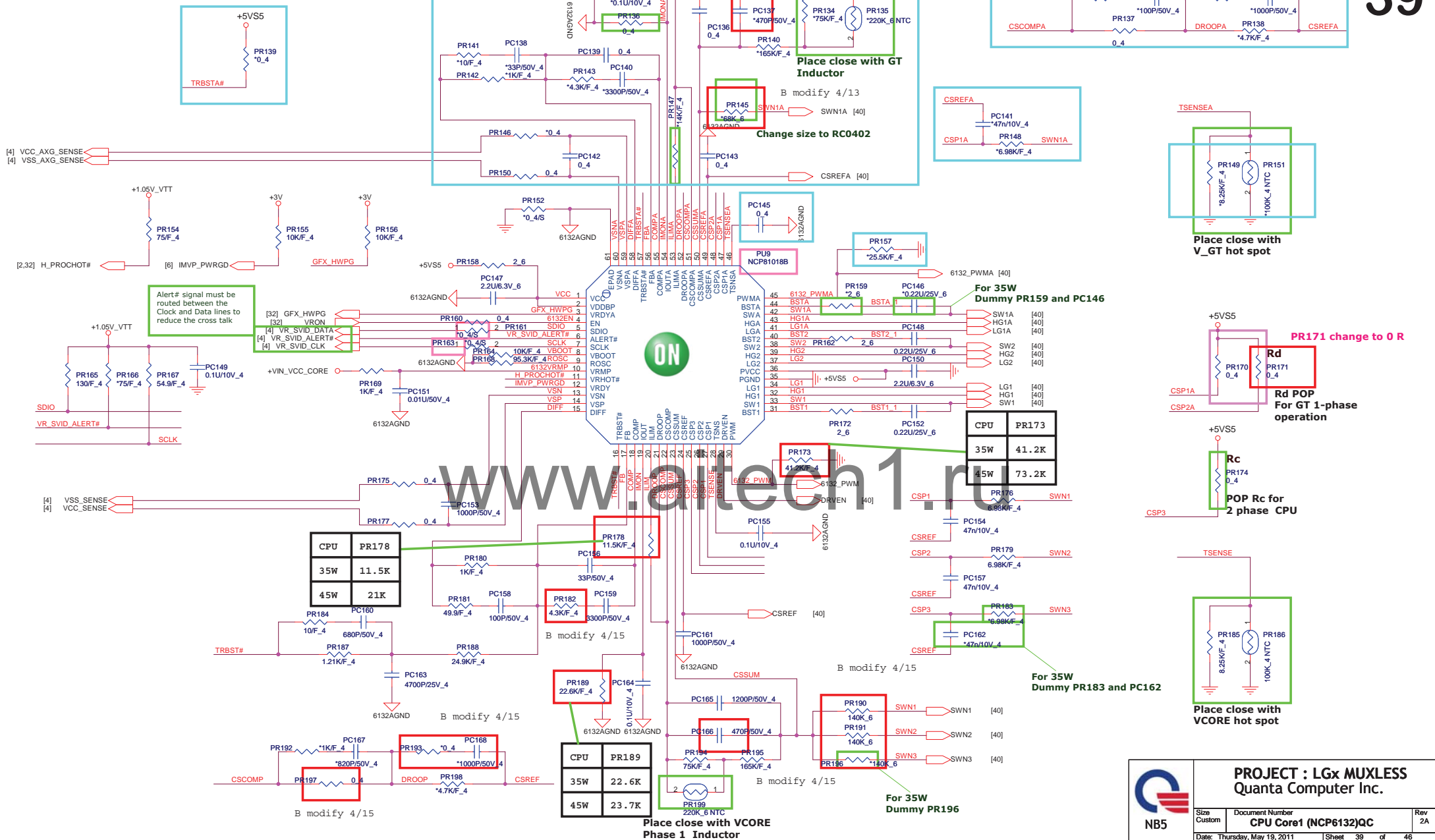
www.aitech1.ru

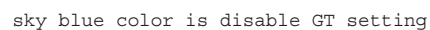


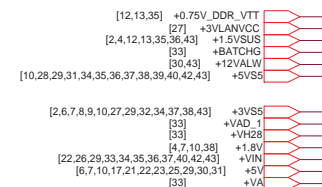


www.aitech1.ru







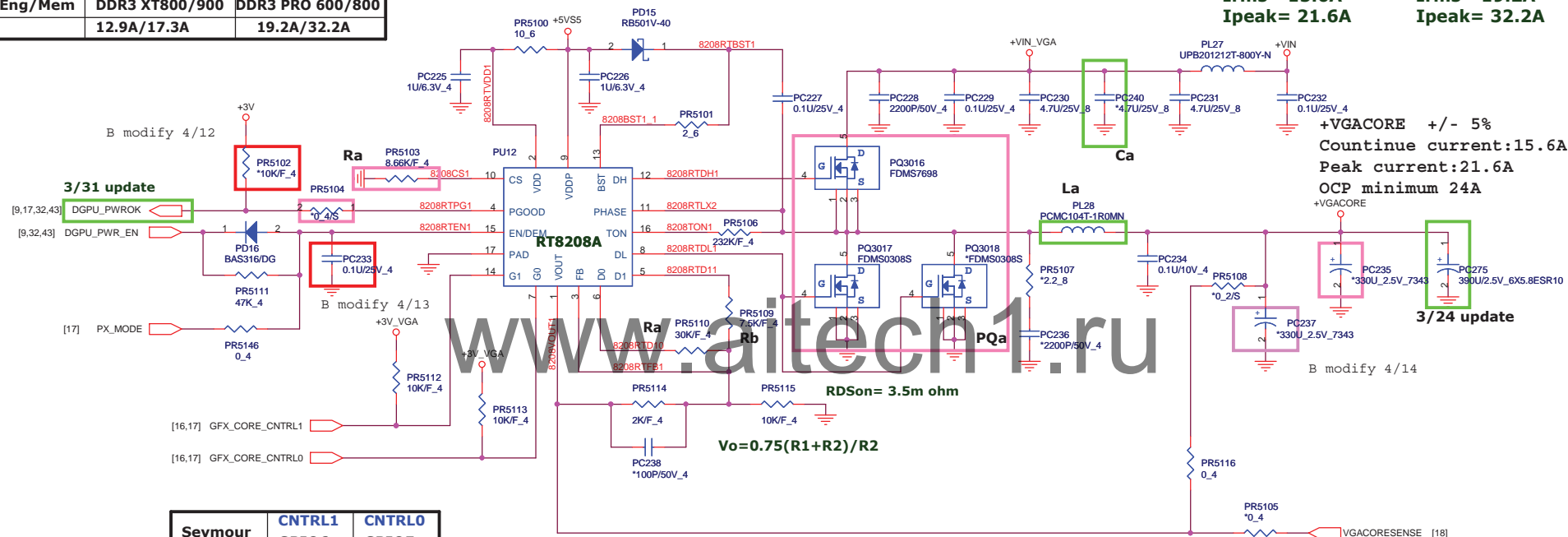


VGA Core

LG2_DIS only
VGA chip only Seymour

42

	Seymour (OCP 24A)	Whistler
Ca	PC240 X	V
Cb	PC235 PC237 X	V
PQa	PQ3018 X	V
La	1U/15A	0.45U25A
Ra	8.66K-ohm	8.66K-ohm
Eng/Mem	DDR3 XT800/900	DDR3 PRO 600/800
	12.9A/17.3A	19.2A/32.2A



Seymour-XT 64bit
Irms= 15.6A
Ipeak= 21.6A

Whistler
Irms= 19.2A
Ipeak= 32.2A

+VGACORE +/- 5%
Countinue current:15.6A
Peak current:21.6A
OCP minimum 24A

$$V_o = 0.75(R_1 + R_2) / R_2$$

Seymour	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
0.95V	0	1
1.1V	1	0
1.15V	1	1

default

Whistler	CNTRL1 GPIO6	CNTRL0 GPIO5
0.9V	0	0
1.0V	0	1
1.05V	1	0
1.15V	1	1

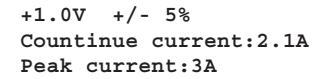
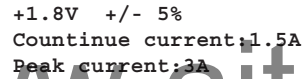
Ra --> 15K-ohm
Rb --> 10K-ohm

[2,6,7,8,9,10,12,13,14,17,21,22,23,24,25,26,27,28,29,30,31,32,37,39,41] +3V
[10,28,29,31,34,35,36,37,38,39,40,41,43] +3V_GFX
[17,18] +5VSS
[22,26,29,33,34,35,36,37,40,41,43] +VIN



PROJECT : LGx MUXLESS
Quanta Computer Inc.

Size Custom Document Number +VGACORE (RT8208) Rev 2A
Date: Wednesday, May 18, 2011 Sheet 42 of 46



Size Custom	Document Number +VGA POWER	Rev 2A
Date: Thursday, May 19, 2011		Sheet 43 of 47

LG2/4 Power rail map

